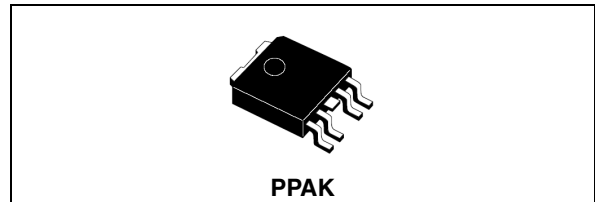


### Features

Type	$R_{DS(on)}$	$I_{out}$	$V_{CC}$
VN751PT	60 m $\Omega$	2.5 A	36 V

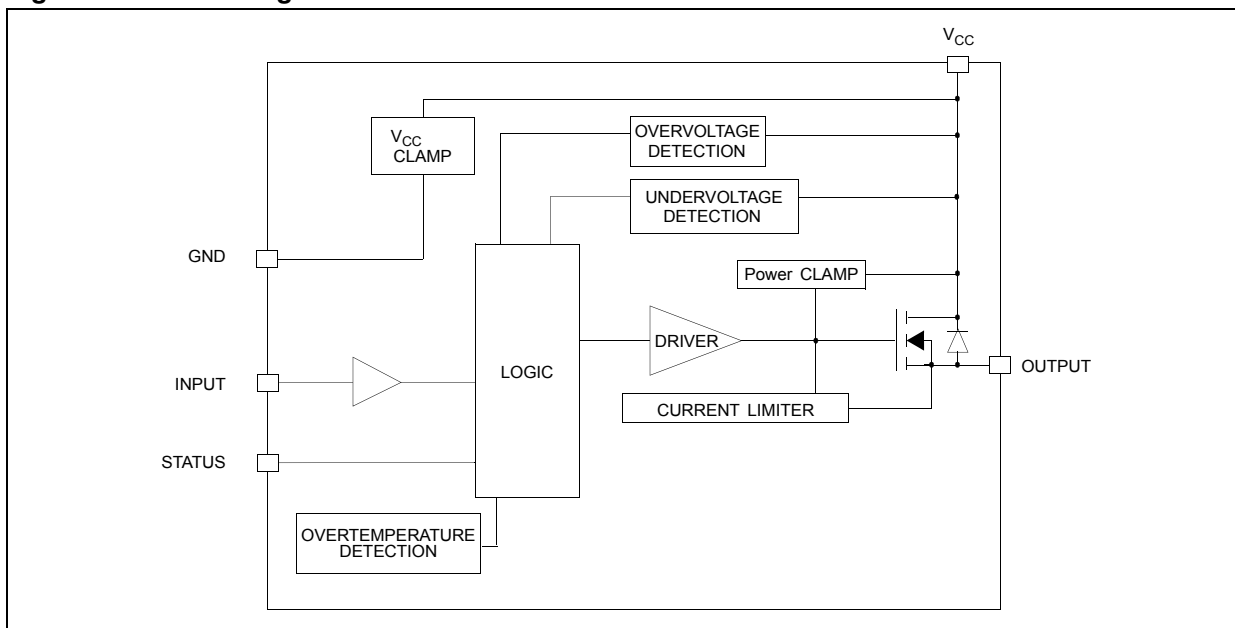
- CMOS compatible input
- Thermal shutdown
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Compliance to 61000-4-4 IEC test up to 4 kV
- Open drain status output



### Description

The VN751PT is a monolithic device designed in STMicroelectronics VIPower M0-3 technology, intended for driving any kind of load with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in conformity with IEC 61131-2 programmable controllers international standard.

**Figure 1. Block diagram**



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# 1 Maximum ratings

**Table 1. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage (overvoltage protected)	45	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-5	A
$I_{IN}$	DC input current	+/- 10	mA
$I_{STAT}$	DC status current	+/- 10	mA
$V_{ESD}$	Electrostatic discharge ( R = 1.5 k $\Omega$ ; C = 100 pF )	5000	V
$P_{tot}$	Power dissipation $T_C = 25\text{ }^{\circ}\text{C}$	Internally limited	W
$T_J$	Junction operating temperature	Internally limited	$^{\circ}\text{C}$
$T_C$	Case operating temperature	- 40 to 150	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
$E_{AS}$	Single-pulse avalanche energy	0.8	J

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}$	Thermal resistance junction-ambient Max	50 <sup>(1)</sup>	$^{\circ}\text{C}/\text{W}$
$R_{thJC}$	Thermal resistance junction-case Max	3	$^{\circ}\text{C}/\text{W}$

1. When mounted on a FR-4 printed circuit board with 0.5 cm<sup>2</sup> of Cu (at least 35 $\mu\text{m}$  thick) connected to all  $V_{CC}$  pins.

## 2 Pin connections

Figure 2. Connection diagram (top view)

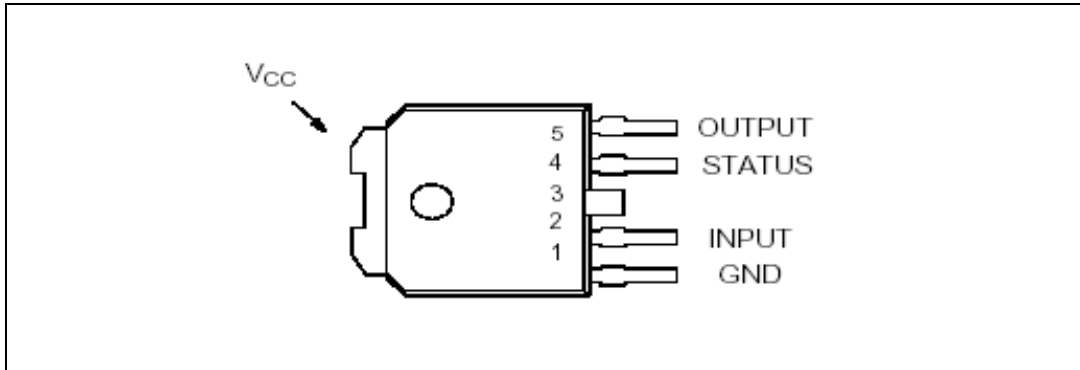
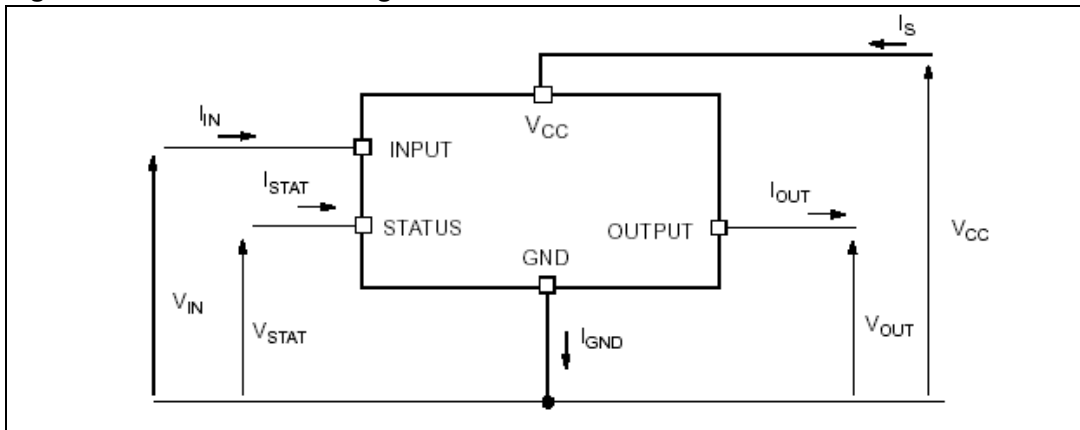


Figure 3. Current and voltage conventions



### 3 Electrical characteristics

$8\text{ V} < V_{CC} < 36\text{ V}$ ;  $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ , unless otherwise specified

**Table 3. Power**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{CC}$	Operating supply voltage		5.5		36	V
$V_{USD}$	Undervoltage shut-down		3	4	5.5	V
$V_{OV}$	Overvoltage shut-down		36			V
$R_{ON}$	On state resistance	$I_{OUT} = 2\text{ A}$ ; $T_J = 25\text{ }^{\circ}\text{C}$ $I_{OUT} = 2\text{ A}$		60	180	mΩ mΩ
$I_S$	Supply current	Off state; $V_{CC} = 24\text{ V}$ ; $T_{CASE} = 25\text{ }^{\circ}\text{C}$ On state; $V_{CC} = 24\text{ V}$ On state; $V_{CC} = 24\text{ V}$ ; $T_{CASE} = 100\text{ }^{\circ}\text{C}$		10 1.5	20	μA mA mA
$I_{L(off)}$	Off state output current	$V_{IN} = V_{OUT} = 0\text{ V}$	0		10	μA

**Table 4. Switching (  $V_{CC} = 24\text{ V}$  )**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 12\text{ }\Omega$ from $V_{IN}$ rising edge to $V_{OUT} = 2.4\text{ V}$		12		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 12\text{ }\Omega$ from $V_{IN}$ falling edge to $V_{OUT} = 21.6\text{ V}$		35		μs
$dV_{OUT}/dt_{(on)}$	Turn -on voltage slope	$R_L = 12\text{ }\Omega$ from $V_{OUT} = 2.4\text{ V}$ to $V_{OUT} = 19.2\text{ V}$		0.80		V/μs
$dV_{OUT}/dt_{(off)}$	Turn -off voltage slope	$R_L = 12\text{ }\Omega$ from $V_{OUT} = 21.6\text{ V}$ to $V_{OUT} = 2.4\text{ V}$		0.30		V/μs

**Table 5. Input pin**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low level				1.25	V
$I_{IL}$	Low level input current	$V_{IN} = 1.25\text{ V}$	1			$\mu\text{A}$
$V_{IH}$	Input high level		3.25			V
$I_{IH}$	High level input current	$V_{IN} = 3.25\text{ V}$			10	$\mu\text{A}$
$V_{hyst}$	Input hysteresis voltage		0.5			V
$I_{IN}$	Input current	$V_{IN} = V_{CC} = 5\text{ V}$			10	$\mu\text{A}$
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1\text{ mA}$ $I_{IN} = -1\text{ mA}$	6	6.8 -0.7	8	V V

**Table 6. Status pin**

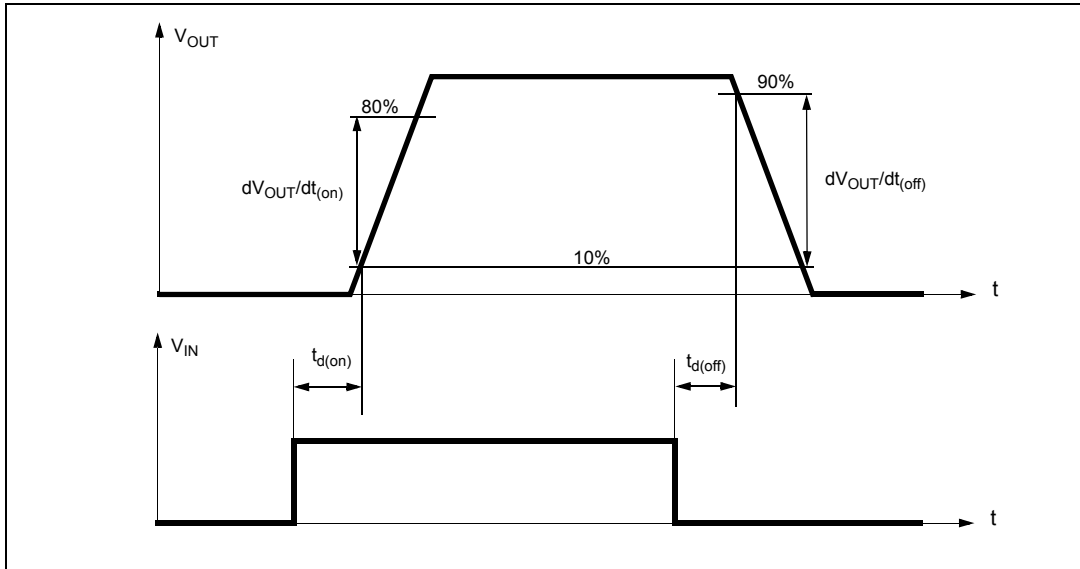
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT} = 1.6\text{ mA}$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT} = 5\text{ V}$			10	$\mu\text{A}$
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			100	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT} = 1\text{ mA}$ ; $I_{STAT} = -1\text{ mA}$	6	6.8 -0.7	8	V V

**Table 7. Protections**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{TSD}$	Shut-down temperature		150	175	200	$^{\circ}\text{C}$
$T_R$	Reset temperature		135			$^{\circ}\text{C}$
$T_{hyst}$	Thermal hysteresis		7	20		$^{\circ}\text{C}$
$I_{lim}$	Current limitation	$V_{CC} = 24\text{ V}$ , $R_{LOAD} = 10\text{ m}\Omega$ , $t = 0.4\text{ ms}$	2.7		6.0	A
$V_{demag}$	Turn-off output clamp voltage	$R_L = 12\ \Omega$ ; $L = 6\text{ mH}$	$V_{CC} - 47$	$V_{CC} - 52$	$V_{CC} - 57$	V

## 4 Waveforms and truth table

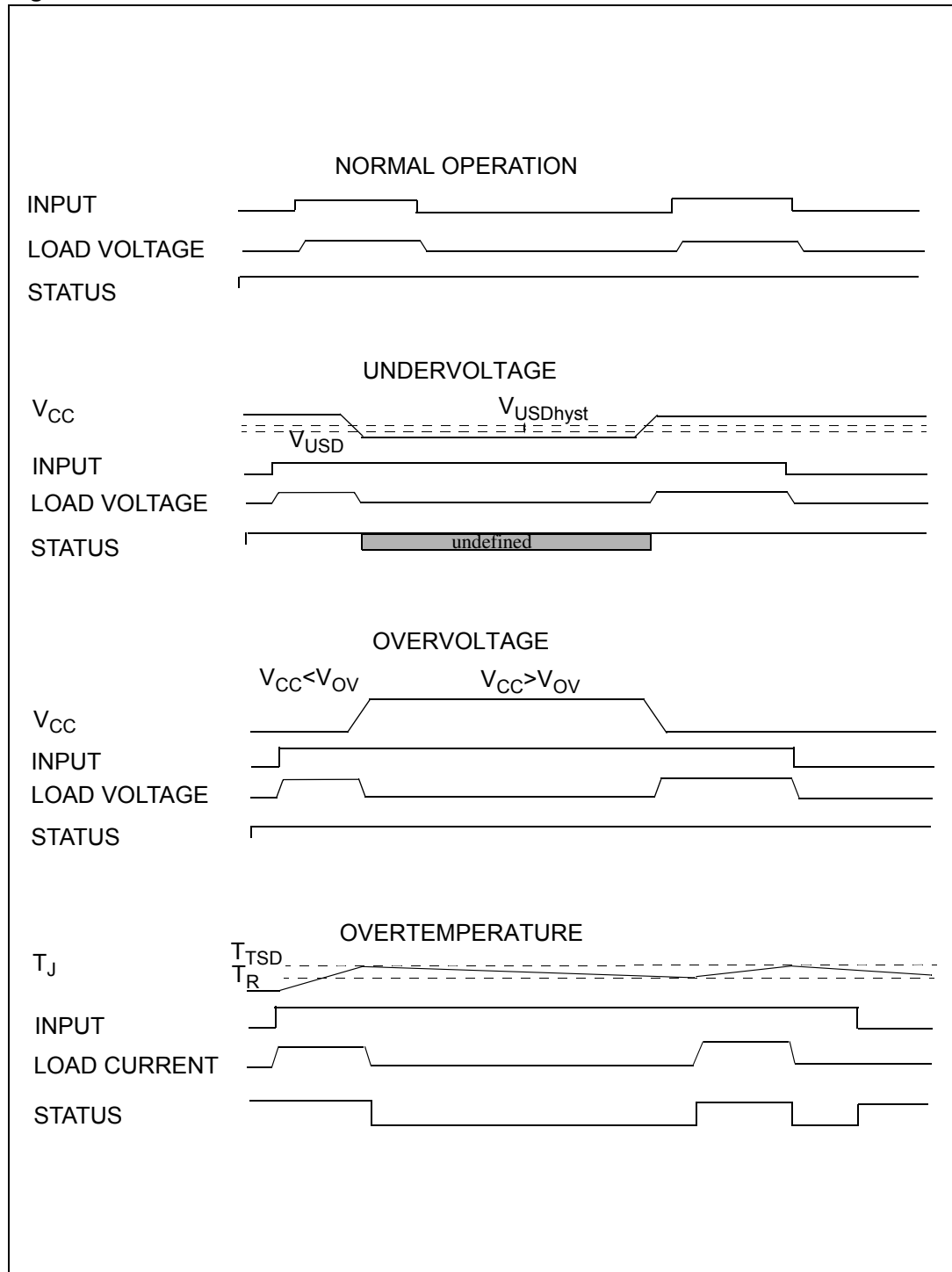
**Figure 4. Switching time waveforms**



**Table 8. Truth table**

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_J < T_{TSD})$ H
	H	X	$(T_J > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

Figure 5. Waveforms





# 5 Test circuit

Figure 6. Peak short circuit current test circuit

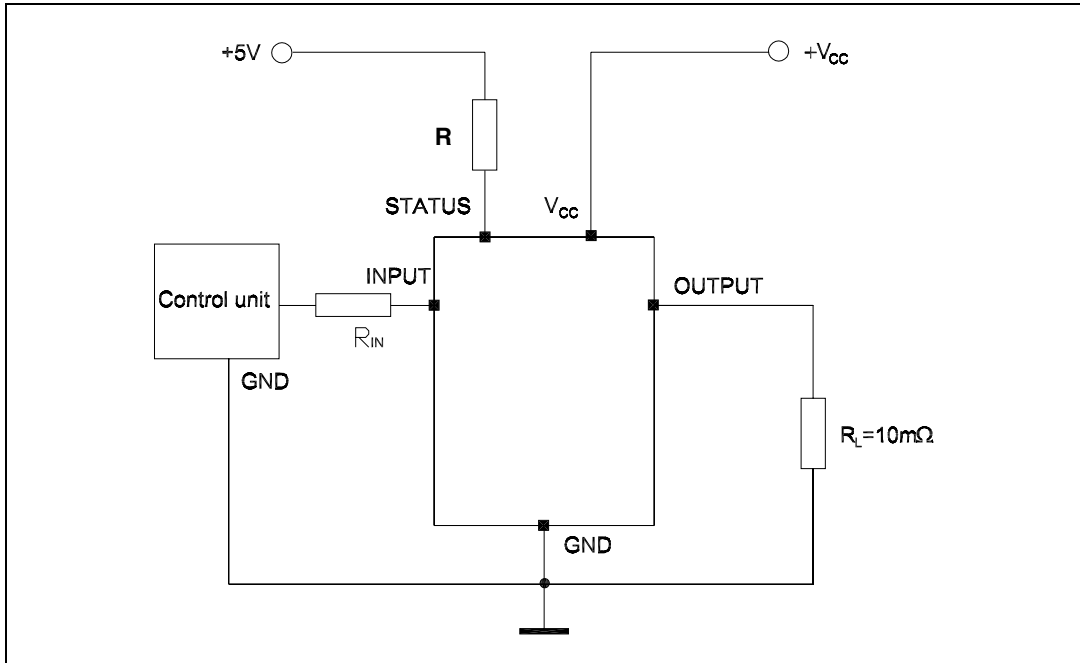
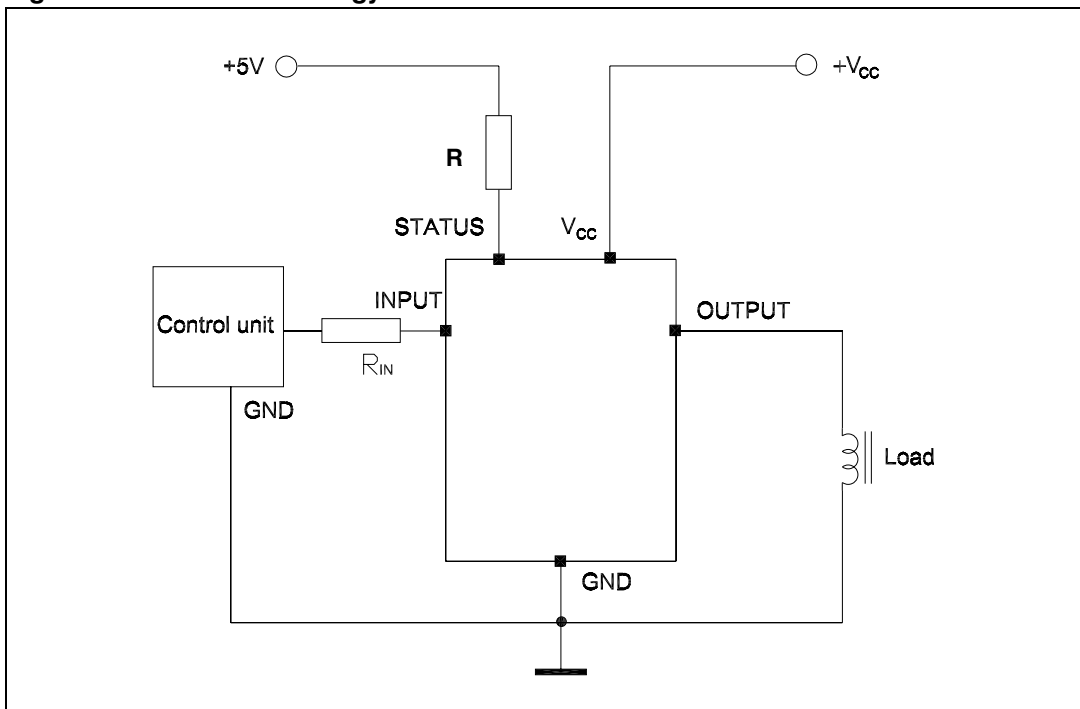
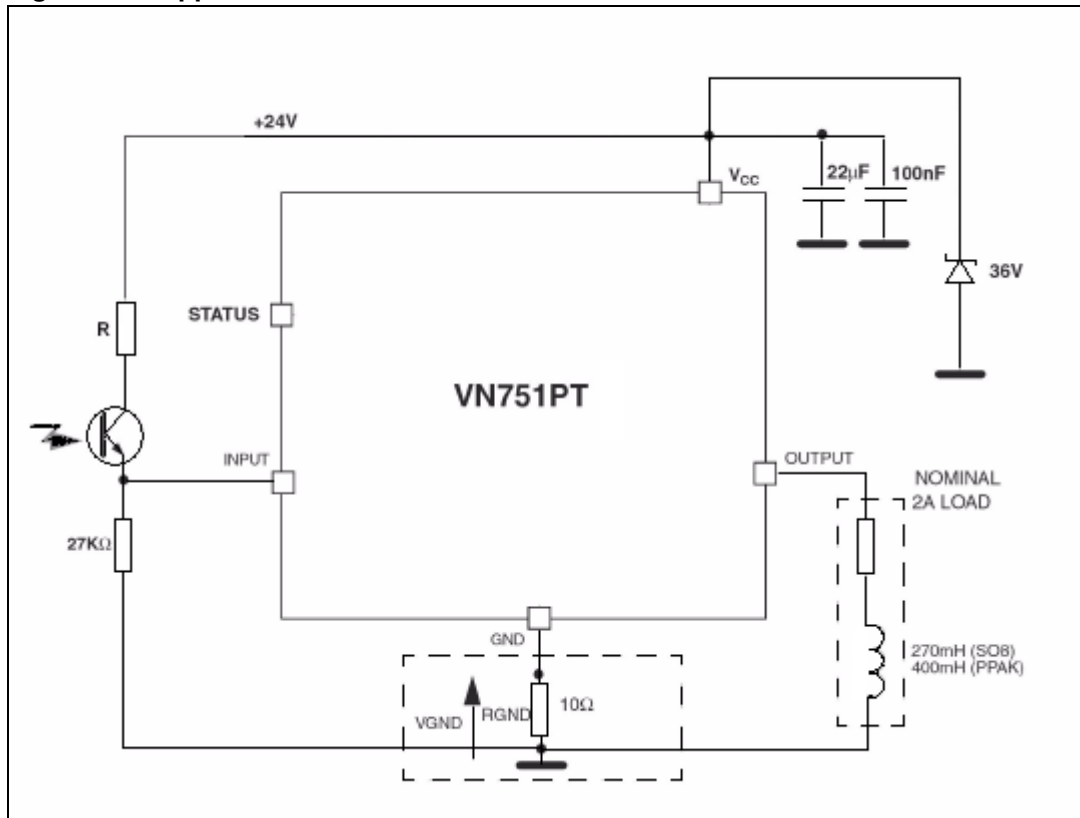


Figure 7. Avalanche energy test circuit



## 6 Application schematic

Figure 8. Application schematic



## 7 Reverse polarity protection

A schematic solution to protect the IC against a reverse polarity condition is proposed.

This schematic is effective with any type of load connected to the outputs of the IC.

The  $R_{GND}$  resistor value can be selected according to the following conditions to be met:

$$R_{GND} \leq 600 \text{ mV} / (I_S \text{ in ON state max}).$$

$$R_{GND} \geq (-V_{CC}) / (-I_{GND})$$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

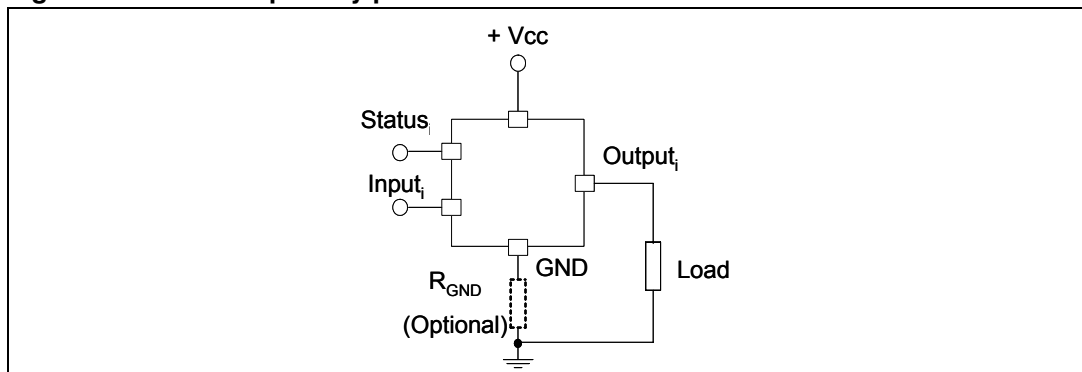
The power dissipation associated to  $R_{GND}$  during reverse polarity condition is:

$$PD = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared by several different ICs. In such case  $I_S$  value on formula (1) is the sum of the maximum ON-state currents of the different devices.

Please note that if the microprocessor ground and the device ground are separated then the voltage drop across the  $R_{GND}$  (given by  $I_S$  in ON state max \*  $R_{GND}$ ) produce a difference between the generated input level and the IC input signal level. This voltage drop will vary depending on how many devices are ON in the case of several high side switches sharing the same  $R_{GND}$ .

**Figure 9. Reverse polarity protection**



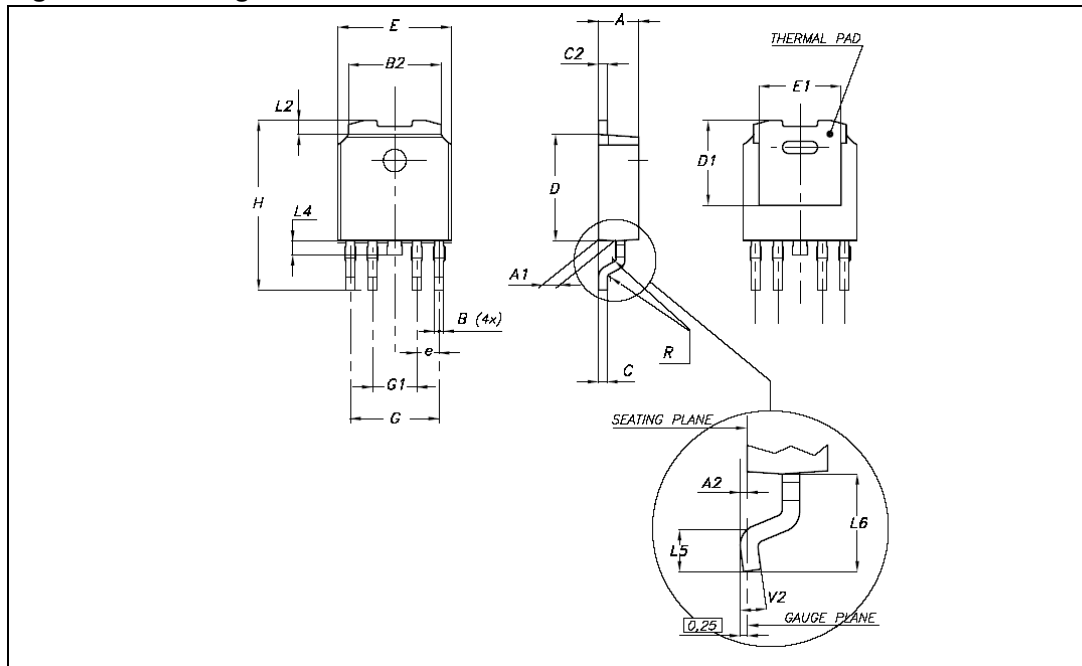
## 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. PPAK mechanical data

Dim.	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0°		8°
Package weight	Gr. 0.3		

Figure 10. Package dimensions



## 9 Order code

**Table 10. Order codes**

<b>Order codes</b>	<b>Package</b>	<b>Packaging</b>
VN751PT	PPAK	Tube
VN751PTTR		Tape and reel

## 10 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
07-Mar-2006	1	Initial release
31-Mar-2006	2	Added $V_{SCL}$
10-Jul-2006	3	Updated $V_{CC}$ value <a href="#">Table 1</a> , $I_{lim}$ min value <a href="#">Table 7</a>
12-Mar-2007	4	Typo in <a href="#">Table 4 on page 5</a> , updated $P_{tot}$ value <a href="#">Table 1</a> .
15-May-2007	5	Typo in <a href="#">Table 1 on page 3</a> , $V_{ESD}$
18-Sep-2007	6	Added $I_{STAT}$ value in <a href="#">Table 1 on page 3</a>
08-Jul-2008	7	Added <a href="#">Section 7 on page 11</a>
30-Nov-2009	8	Updated coverpage and <a href="#">Chapter 6 on page 10</a>



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