



VINCULUM

BINDING USB TECHNOLOGIES

Future Technology Devices International Ltd.

V2DIP2-32

VNC2-32Q Development Module Datasheet

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Future Technology Devices International Ltd (FTDI)

Unit 1, 2 Seaward Place, Centurion Business Park, Glasgow, G41 1HH, United Kingdom

Tel.: +44 (0) 141 429 2777 Fax: + 44 (0) 141 429 2758

E-Mail (Support): support1@ftdichip.com

Web: <http://www.vinculum.com>

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1 Introduction

V2DIP2-32 module is designed to allow rapid development of designs using the VNC2-32Q IC. The V2DIP2-32 is supplied as a PCB designed to fit into a 24 pin 0.6" wide 0.1"pitch DIP socket. The module provides access to the UART, parallel FIFO, and SPI interface pins of the VNC2-32Q device, via its IO bus pins. Two USB ports are accessed via type A USB connectors.

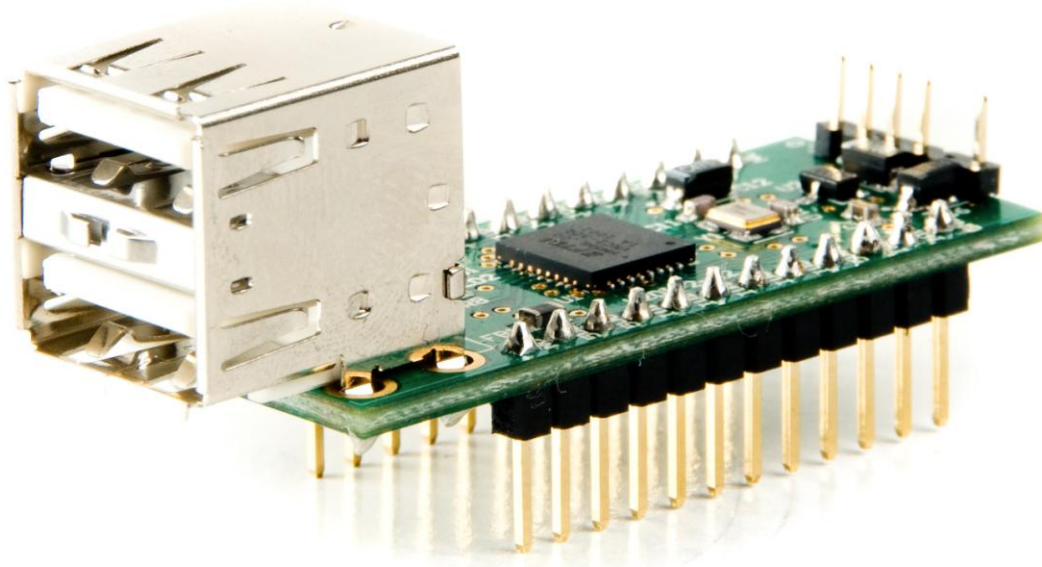


Figure 1.1 - V2DIP2-32

The VNC2 is the second of FTDI's Vinculum family of Embedded dual USB host controller devices. The VNC2 device provides USB Host interfacing capability for a variety of different USB device classes including support for BOMS (bulk only mass storage), Printer, HID (human interface devices). For mass storage devices such as USB Flash drives, VNC2 also transparently handles the FAT file structure.

Communication with non USB devices such as a low cost microcontroller is accomplished via either UART, SPI or parallel FIFO interfaces. The VNC2 provides a new cost effective solution for providing USB Host capability into products that previously did not have the hardware resources available.

The VNC2 supports the capability to enable customers to develop custom firmware using the Vinculum II development software tool suite. The development tools support compiler, linker and debugger tools complete within an integrated development environment (IDE).

The Vinculum-II VNC2 family of devices are available in Pb-free (RoHS compliant) 32-lead LQFP, 32-lead QFN, 48-lead LQFP, 48-lead QFN, 64-Lead IQFP and 64-lead QFN packages

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2 Features

The V2DIP2-32 incorporates the following features:

- Uses FTDI's the VNC2-32Q embedded USB host controller IC device
- Two USB 'A' type socket to interface with USB peripheral devices
- UART, parallel FIFO and SPI interfaces can be programmed to a choice of available I/O pins
- Single 5V supply input from DIL connectors or 5V supplied via USB VBUS slave interface or debugger module.
- Auxiliary 3.3 V / 200 mA power output to external logic
- Power and traffic indicator LED's
- All VNC2 signals available on 0.6" wide / 0.1" pitch DIL male connectors.
- V2DIP2-32 is a Pb-free, RoHS complaint development module
- Debugger interface pin available on DIL pins or via 6 way male header which interfaces to separate debugger module
- Firmware upgrades via UART or debugger interface pin header
- FOC software development suite of tools to create customised firmware includes a Compiler, Linker, Debugger and Assembler all wrapped up in an easy to use Integrated Design Environment GUI.

3 Pin Out and Signal Description

3.1 Module Pin Out

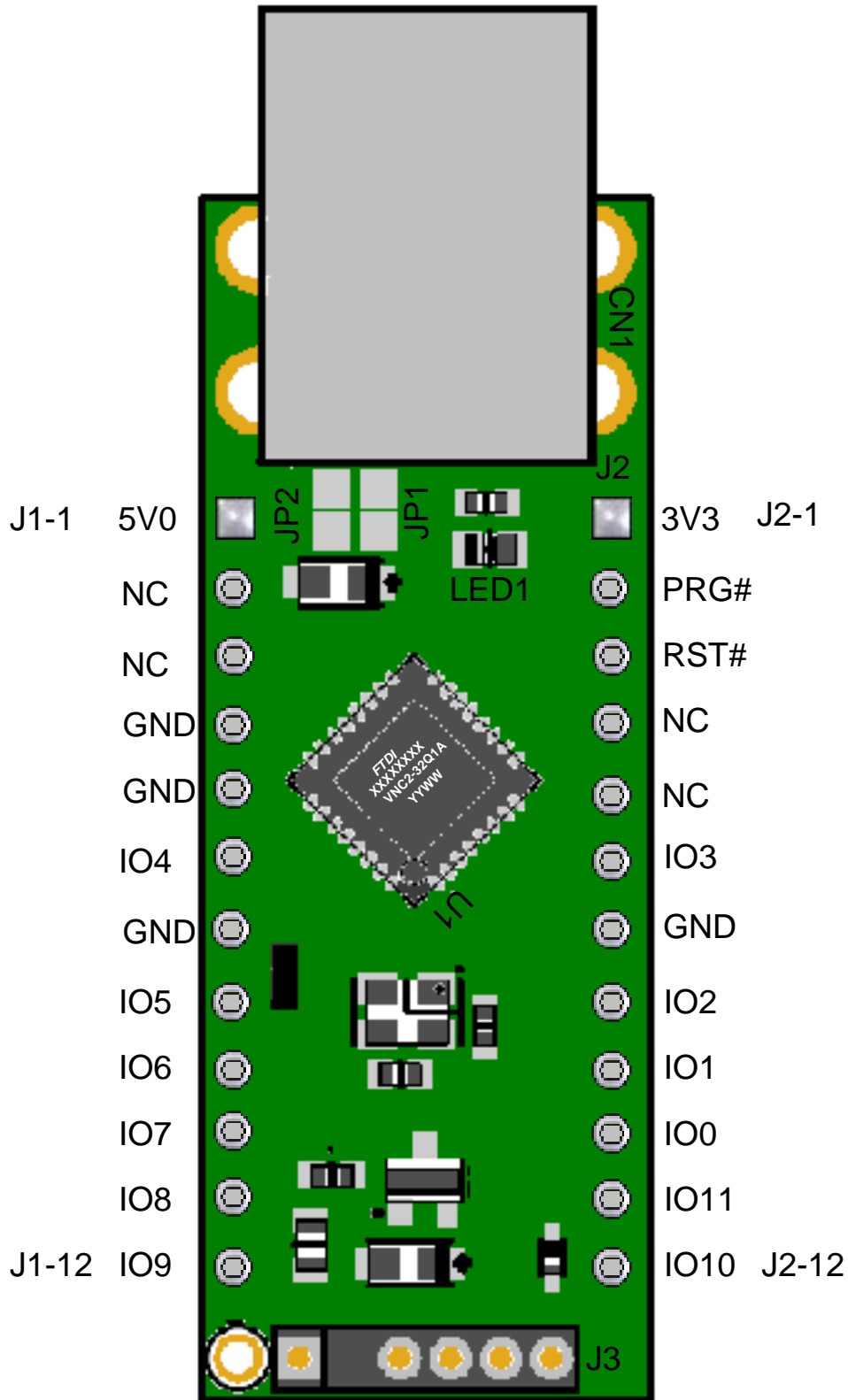


Figure 3.1 - V2DIP2-32 Module Pin Out (Top View)

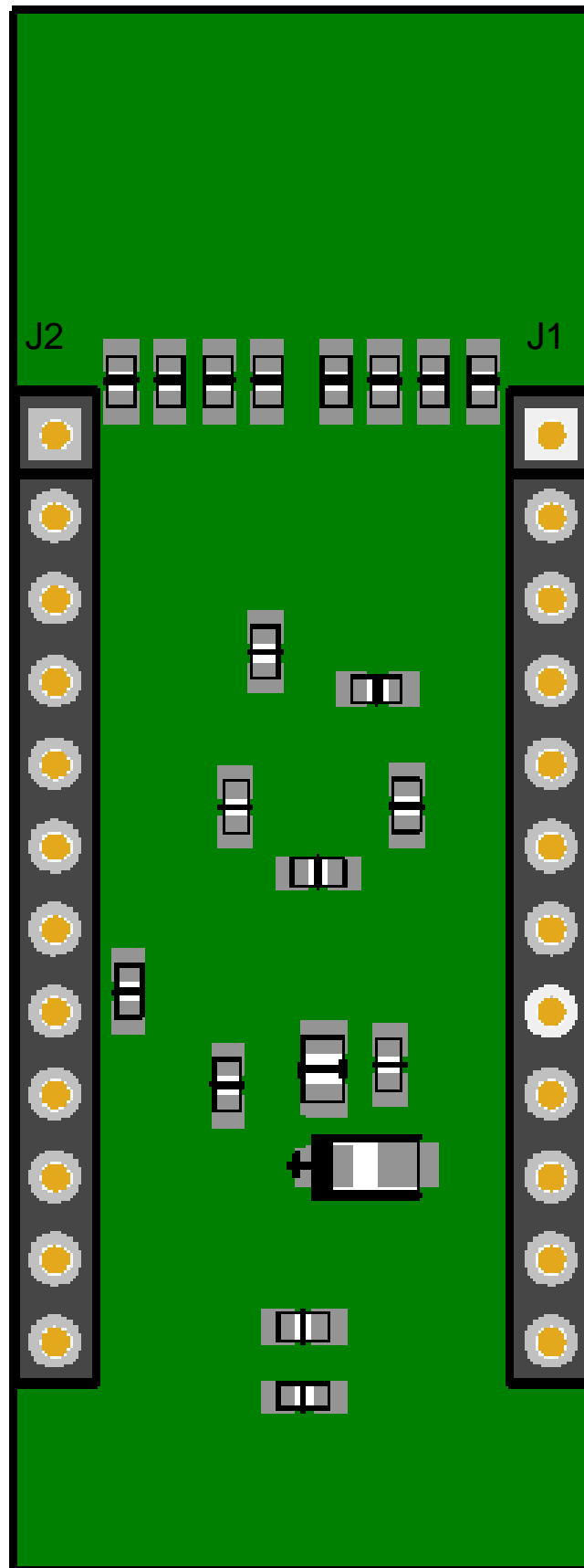


Figure 3.2 - V2DIP2-32 Module Pin Out (Bottom View)

3.2 Pin Signal Description

| <i>Pin No.</i> | <i>Name</i> | <i>Pin Name on PCB</i> | <i>Type</i> | <i>Description</i> |
|----------------|-------------|------------------------|---|--|
| J1-1 | 5V0 | 5V0 | PWR Input | 5.0V module supply pin. This pin can be used to provide the 5.0V input to the V2DIP2-64 when the V2DIP2-64 is not powered from the USB connector (VBUS) or the debugger interface. Also connected to DIL connector pins J1-1 and J3-6. |
| J1-2 | - | - | - | Not connected |
| J1-3 | - | - | - | Not connected |
| J1-4 | GND | GND | PWR | Module ground supply pin |
| J1-5 | GND | GND | PWR | Module ground supply pin |
| J1-6 | IOBUS4 | IO4 | I/O | 5V safe bidirectional data / control bus bit 4 |
| J1-7 | GND | GND | PWR | Module ground supply pin |
| J1-8 | IOBUS5 | IO5 | I/O | 5V safe bidirectional data / control bus bit 5 |
| J1-9 | IOBUS6 | IO6 | I/O | 5V safe bidirectional data / control bus bit 6 |
| J1-10 | IOBUS7 | IO7 | I/O | 5V safe bidirectional data / control bus bit 7 |
| J1-11 | IOBUS8 | IO8 | I/O | 5V safe bidirectional data / control bus bit 8 |
| J1-12 | IOBUS9 | IO9 | I/O | 5V safe bidirectional data / control bus bit 9 |
| J2-1 | 3V3 | 3V3 | 3.3V Output from VDIP2's on board 3.3V L.D.O. | 3.3V output from V2DIP2's on board 3.3V L.D.O. |
| J2-2 | PROG# | PRG# | Input | This pin is used in combination with the RESET# pin and the UART interface to program firmware into the VNC2. |
| J2-3 | RESET# | RST# | Input | Can be used by an external device to reset the VNCL2. This pin is also used in combination with PROG# and the UART interface to program firmware into the VNC2 |
| J1-4 | - | - | - | Not connected |
| J1-5 | - | - | - | Not connected |
| J2-6 | IOBUS3 | IO3 | I/O | 5V safe bidirectional data / control bus bit 3 |
| J2-7 | GND | GND | PWR | Module ground supply pin |
| J2-8 | IOBUS2 | IO2 | I/O | 5V safe bidirectional data / control bus bit 2 |
| J2-9 | IOBUS1 | IO1 | I/O | 5V safe bidirectional data / control bus bit 1 |
| J2-10 | IOBUS0 | IO0 | I/O | 5V safe bidirectional data / control bus bit 0 |
| J2-11 | IOBUS11 | IO11 | I/O | 5V safe bidirectional data / control bus bit 11 |
| J2-12 | IOBUS10 | IO10 | I/O | 5V safe bidirectional data / control bus bit 10 |

Table 3.1 - Pin Signal Descriptions

3.3 Default Interface I/O Pin Configuration

The 32 pin QFN VNC2-32Q device is delivered without any firmware pre-loaded. As such the IOMUX will provide a default pinout as shown in **Table 3.2**

| Pin No. | Pin Name on PCB | Type | Data and Control Bus Configuration Options | | | | |
|---------|-----------------|------|--|---------------------|----------------------|-------------------------|--------------------|
| | | | UART Interface | SPI Slave Interface | SPI Master Interface | Parallel FIFO Interface | Debugger Interface |
| J2-10 | IO0 | I/O | NA | NA | NA | NA | Debug_if |
| J1-6 | IO4 | I/O | uart_txd | NA | NA | NA | NA |
| J1-8 | IO5 | I/O | uart_rxd | NA | NA | NA | NA |
| J1-9 | IO6 | I/O | uart_rts# | NA | NA | NA | NA |
| J1-10 | IO7 | I/O | uart_cts# | NA | NA | NA | NA |
| J1-11 | IO8 | I/O | NA | spi_s0_clk | NA | NA | NA |
| J1-12 | IO9 | I/O | NA | spi_s0_mosi | NA | NA | NA |
| J2-12 | IO10 | I/O | NA | spi_s0_miso | NA | NA | NA |
| J2-11 | IO11 | I/O | NA | spi_s0_ss# | NA | NA | NA |

Table 3.2 - Default Interface I/O Pin Configuration

3.4 UART Interface

When the data and control buses are configured in UART mode, the interface implements a standard asynchronous serial UART port with flow control. The UART can support baud rates from 300baud to 3Mbaud. The UART interface is described more fully in a Vinculum-II datasheet please refer to:- [FTDI website](#)

3.4.1 Signal Description – UART Interface

The UART signals can be programmed to a choice of available I/O pins. **Table 3.3** explains the available pins for each of the UART signals.

| <i>Available Pins</i> | <i>Name</i> | <i>Type</i> | <i>Description</i> |
|-----------------------|----------------|-------------|---|
| J2-10, J1-6, J1-11 | uart_txd | Output | Transmit asynchronous data output |
| J2-9, J1-8, J1-12 | uart_rxd | Input | Receive asynchronous data input |
| J2-8, J1-9, J2-12 | uart_rts# | Output | Request To Send Control Output |
| J2-6, J1-10, J2-11 | uart_cts# | Input | Clear To Send Control Input |
| J2-10, J1-6, J1-11 | uart_dtr# | Output | Data Acknowledge (Data Terminal Ready Control) Output |
| J2-9, J1-8, J1-12 | uart_dsr# | Input | Data Request (Data Set Ready Control) Input |
| J2-8, J1-9, J2-12 | uart_dcd# | Input | Data Carrier Detect Control Input |
| J2-6, J1-10, J2-11 | uart_ri# | Input | Ring Indicator Control Input. RI# low can be used to resume the PC USB Host controller from suspend. |
| J2-10, J1-6, J1-11 | uart_tx_active | Output | Enable Transmit Data for RS485 designs. TXDEN may be used to signal that a transmit operation is in progress. The TXDEN signal will be set high one bit-time before data is transmitted and return low one bit time after the last bit of a data frame has been transmitted |

Table 3.3 - Data and Control Bus Signal Mode Options – UART

3.5 Serial Peripheral Interface (SPI)

The VNC2-32Q has one master module and two slave modules. These modules are described more fully in a VNC2 datasheet please refer to:- [FTDI website](#)

3.5.1 Signal Description - SPI Slave

The SPI Slave signals can be programmed to a choice of available I/O pins. **Table 3.4** explains the available pins for each of the SPI Slave signals.

| <i>Available Pins</i> | <i>Name</i> | <i>Type</i> | <i>Description</i> |
|-----------------------|----------------------------|--------------|--|
| J2-10, J1-6, J1-11 | spi_s0_clk spi_s1_clk | Input | Slave clock input |
| J2-9, J1-8, J1-12 | spi_s0_mosi spi_s1_mosi | Input/Output | Master Out Slave In Synchronous data from master to slave |
| J2-8, J1-9, J2-12 | spi_s0_miso spi_s1_miso | Output | Master In Slave Out Synchronous data from slave to master |
| J2-6, J1-10, J2-11 | spi_s0_ss# spi_s1_ss# | Input | Slave chip select |

Table 3.4 - Data and Control Bus Signal Mode Options – SPI Slave

3.5.2 Signal Description - SPI Master

The SPI Master signals can be programmed to a choice of available I/O pins. **Table 3.5** shows the SPI master signals and the available pins that they can be mapped.

| <i>Available Pins</i> | <i>Name</i> | <i>Type</i> | <i>Description</i> |
|-----------------------|-------------|-------------|--|
| J2-10, J1-6, J1-11 | spi_m_clk | Output | SPI master clock input |
| J2-9, J1-8, J1-12 | spi_m_mosi | Output | Master Out Slave In Synchronous data from master to slave |
| J2-8, J1-9, J2-12 | spi_m_miso | Input | Master In Slave Out Synchronous data from slave to master |
| J2-6, J1-10, J2-11 | spi_m_ss_0# | Output | Active low slave select 0 from master to slave 0 |
| J2-10, J1-6, J1-11 | spi_m_ss_1# | Output | Active low slave select 1 from master to slave 1 |

Table 3.5 - Data and Control Bus Signal Mode Options – SPI Master

3.6 Parallel FIFO Interface - Asynchronous Mode

The Parallel FIFO Asynchronous mode is functionally the same as the Parallel FIFO Interface present in VDIP1 has an eight bit data bus, individual read and write strobes and two hardware flow control signals.

3.6.1 Signal Description - Parallel FIFO Interface

The Parallel FIFO Interface signals can be programmed to a choice of available I/O pins. **Table 3.6** shows the Parallel FIFO Interface signals and the pins that they can be mapped.

| <i>Available Pins</i> | <i>Name</i> | <i>Type</i> | <i>Description</i> |
|-----------------------|--------------|-------------|--|
| J2-10, J1-6, J1-11 | fifo_data[0] | I/O | FIFO data bus Bit 0 |
| J2-9, J1-8, J1-12 | fifo_data[1] | I/O | FIFO data bus Bit 1 |
| J2-8, J1-9, J2-12 | fifo_data[2] | I/O | FIFO data bus Bit 2 |
| J2-6, J1-10, J2-11 | fifo_data[3] | I/O | FIFO data bus Bit 3 |
| J2-10, J1-6, J1-11 | fifo_data[4] | I/O | FIFO data bus Bit 4 |
| J2-9, J1-8, J1-12 | fifo_data[5] | I/O | FIFO data bus Bit 5 |
| J2-8, J1-9, J2-12 | fifo_data[6] | I/O | FIFO data bus Bit 6 |
| J2-6, J1-10, J2-11 | fifo_data[7] | I/O | FIFO data bus Bit 7 |
| J2-10, J1-6, J1-11 | fifo_rxf# | Output | When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high. |
| J2-9, J1-8, J1-12 | fifo_txe# | Output | When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low. |
| J2-8, J1-9, J2-12 | fifo_rd# | Input | Enables the current FIFO data byte on D0...D7 when low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low |
| J2-6, J1-10, J2-11 | fifo_wr# | Input | Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low. |

Table 3.6 - Data and Control Bus Signal Mode Options – Parallel FIFO Interface

3.6.2 Timing Diagram – Asynchronous FIFO Mode Read and Write Cycle

When in Asynchronous FIFO interface mode, the timing of a read and write operation on the FIFO interface is shown in Figure 3.3 and Table 3.7

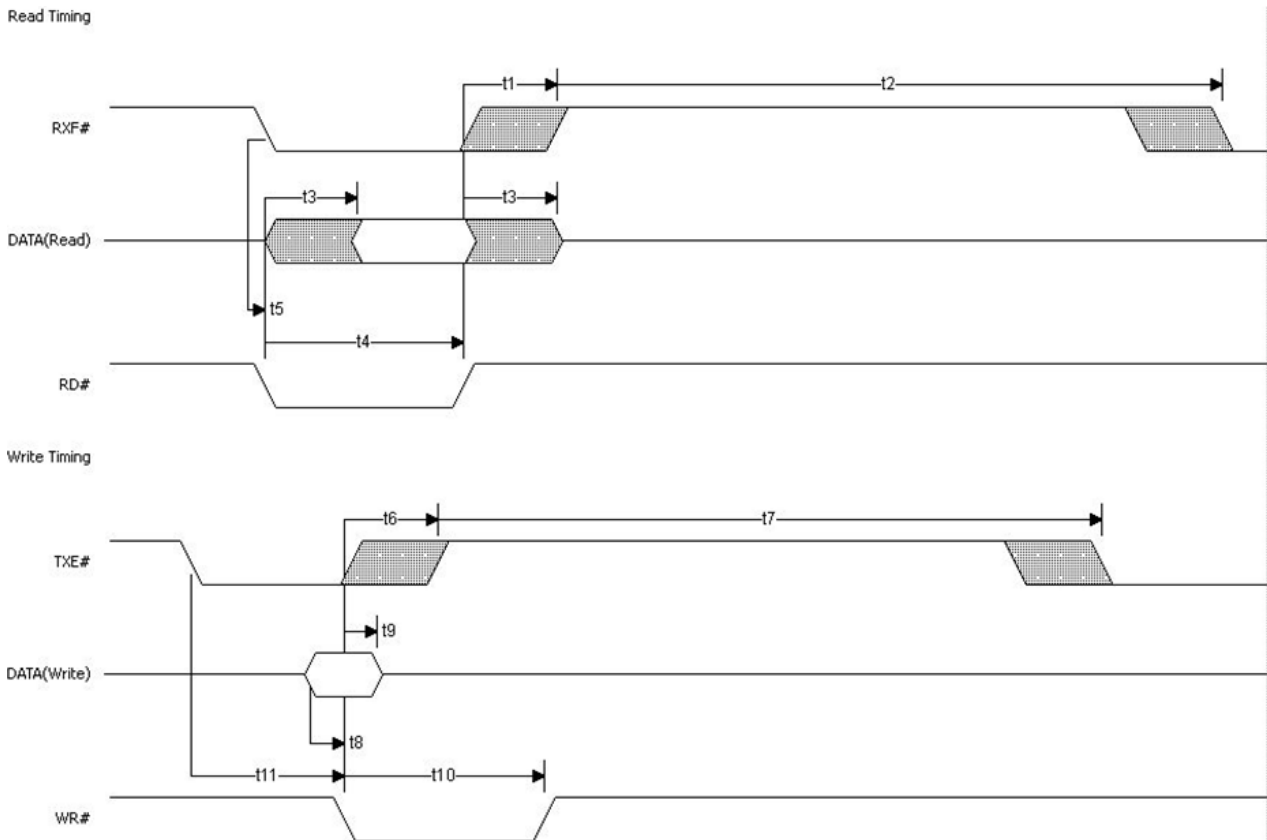


Figure 3.3 – Asynchronous FIFO Mode Read and Write Cycle.

| Time | Description | Min | Max | Unit |
|------|-----------------------------------|-----|-----|------|
| t1 | RD# inactive to RXF# | 1 | 14 | ns |
| t2 | RXF# inactive after RD# cycle | 100 | - | ns |
| t3 | RD# to Data | 1 | 14 | ns |
| t4 | RD# active pulse width | 30 | - | ns |
| t5 | RD# active after RXF# | 0 | - | ns |
| t6 | WR# active to TXE# inactive | 1 | 14 | ns |
| t7 | TXE# inactive after WR# cycle | 100 | - | ns |
| t8 | DATA to TXE# active setup time | 5 | - | ns |
| t9 | DATA hold time after WR# inactive | 5 | - | ns |
| t10 | WR# active pulse width | 30 | - | ns |
| t11 | WR# active after TXE# | 0 | - | ns |

Table 3.7 - Asynchronous FIFO Mode Read Cycle Timing

In asynchronous mode an external device can control data transfer driving FIFO_WR# and FIFO_RD# inputs.

Current byte is available to be read when FIFO_RD# goes low. When FIFO_RD# goes high, FIFO_RXF# output will also go high. It will only become low again when there is another byte to read.

When FIFO_WR# goes low FIFO_TXE# flag will always go high. FIFO_TXE# goes low again only when there is still space for data to be written in to the module.

3.7 Debugger Interface

The purpose of the debugger interface is to provide access to the VNC2 silicon/firmware debugger. The debug interface can be accessed via the J2-10 pin on the DIL connector or, more easily, it can be accessed by connecting a *VNC2_Debug_Module* to the J3 connector. This debug module will give access to the debugger through a USB connection to a PC via the Integrated Development Environment (IDE). The IDE is a graphical interface to the VNC2 software development tool-chain and gives the following debug capabilities through the debugger interface:

- Flash Erase, Write and Program.
- Application debug - application code can have breakpoints, be single stepped and can be halted.
- Detailed internal debug - memory and register read/write access.

The Debugger Interface, and how to use it, is further described in the following applications Note [Vinculum-II Debug Interface Description](#)

3.7.1 Signal Description - Debugger Interface

Table 3.8 shows the signals and pins description for the Debugger Interface pin header J3

| <i>Pin No.</i> | <i>Name</i> | <i>Name On PCB</i> | <i>Type</i> | <i>Description</i> |
|----------------|-------------|--------------------|-------------|--|
| J3-1 | I00 | DBG | I/O | Debugger Interface |
| J3-2 | - | [Key] | - | Not connected. Used to make sure that the debug module is connected correctly. |
| J3-3 | GND | GND | PWR | Module ground supply pin |
| J3-4 | RESET# | RST# | Input | Can be used by an external device to reset the VNCL2. This pin is also used in combination with PROG# and the UART interface to program firmware into the VNC2. |
| J3-5 | PROG# | PRG# | Input | This pin is used in combination with the RESET# pin and the UART interface to program firmware into the VNC2. |
| J3-6 | 5V0 | VCC | PWR Input | 5.0V module supply pin. This pin can be used to provide the 5.0V input to the V2DIP2-32 from the debugger interface when the V2DIP2-32 is not powered from the USB connector (VBUs) or the DIL connector pins J1-1 and J3-6. |

Table 3.8 - Signal Name and Description – Debugger Interface

4 Firmware

4.1 Firmware Support

The VNC2 on the V2DIP2-32 can be programmed with the customers own firmware created using the Vinculum II firmware development tool chain or with various pre-compiled firmware profiles to allow a designer to easily change the functionality of the chip. Please refer to:- [FTDI website](#) for full details on available pre-compiled firmware

4.2 Available Firmware

V2DAP firmware is currently available: USB Host for single Flash Disk and general purpose USB peripherals. Selectable UART, FIFO or SPI interface command monitor. please refer to:- [FTDI website](#) for full details.

4.3 Firmware Upgrades

Refer to the debugger interface section which can be used to update the firmware..

5 Mechanical Dimensions

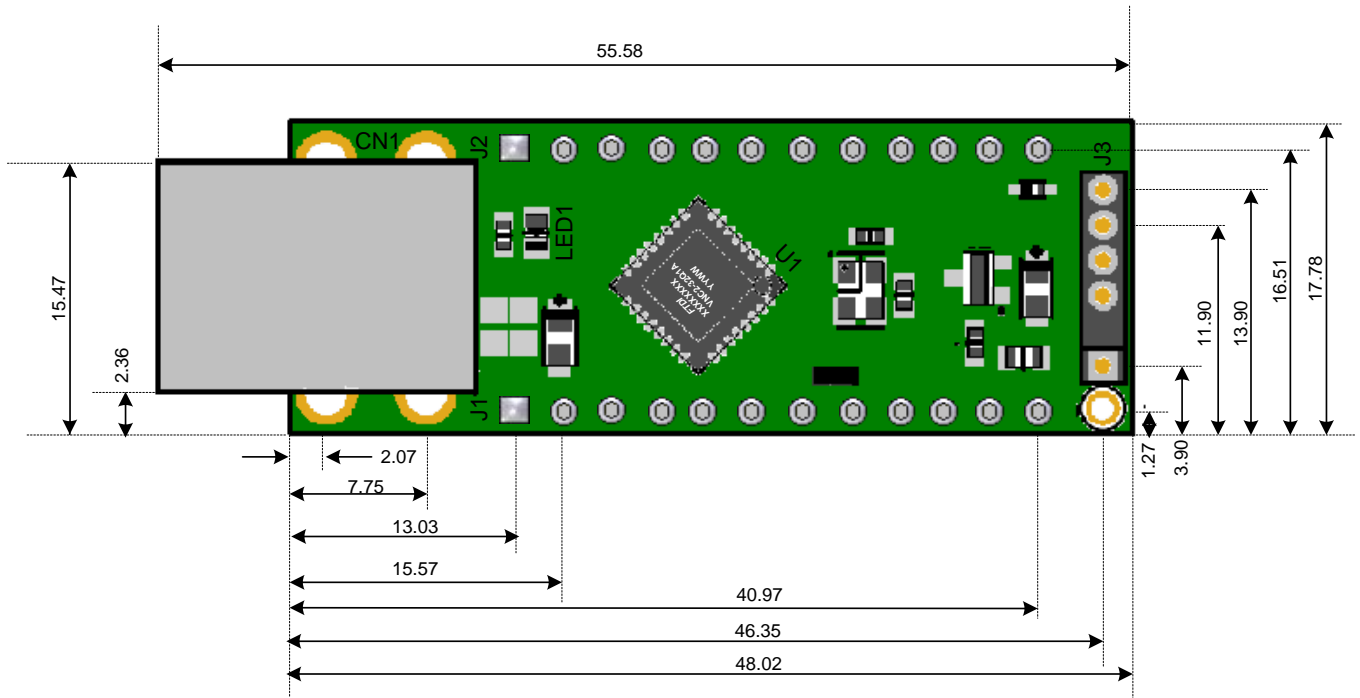


Figure 5.1 - V2DIP2-32 Dimensions (Top View)

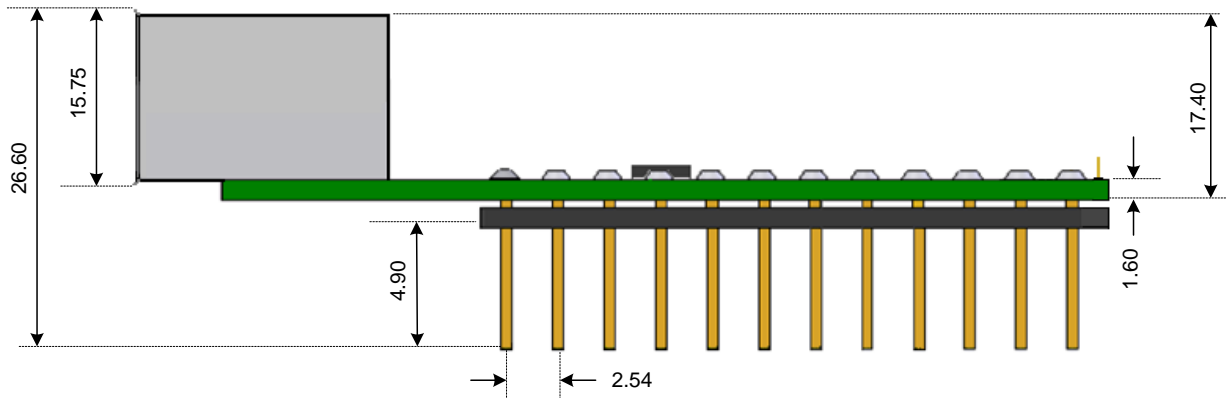


Figure 5.2 - V2DIP2-32 Dimensions (Side View)

±0.20mm Tolerance (except pitch)

All dimensions are in mm

6 Schematic Diagram

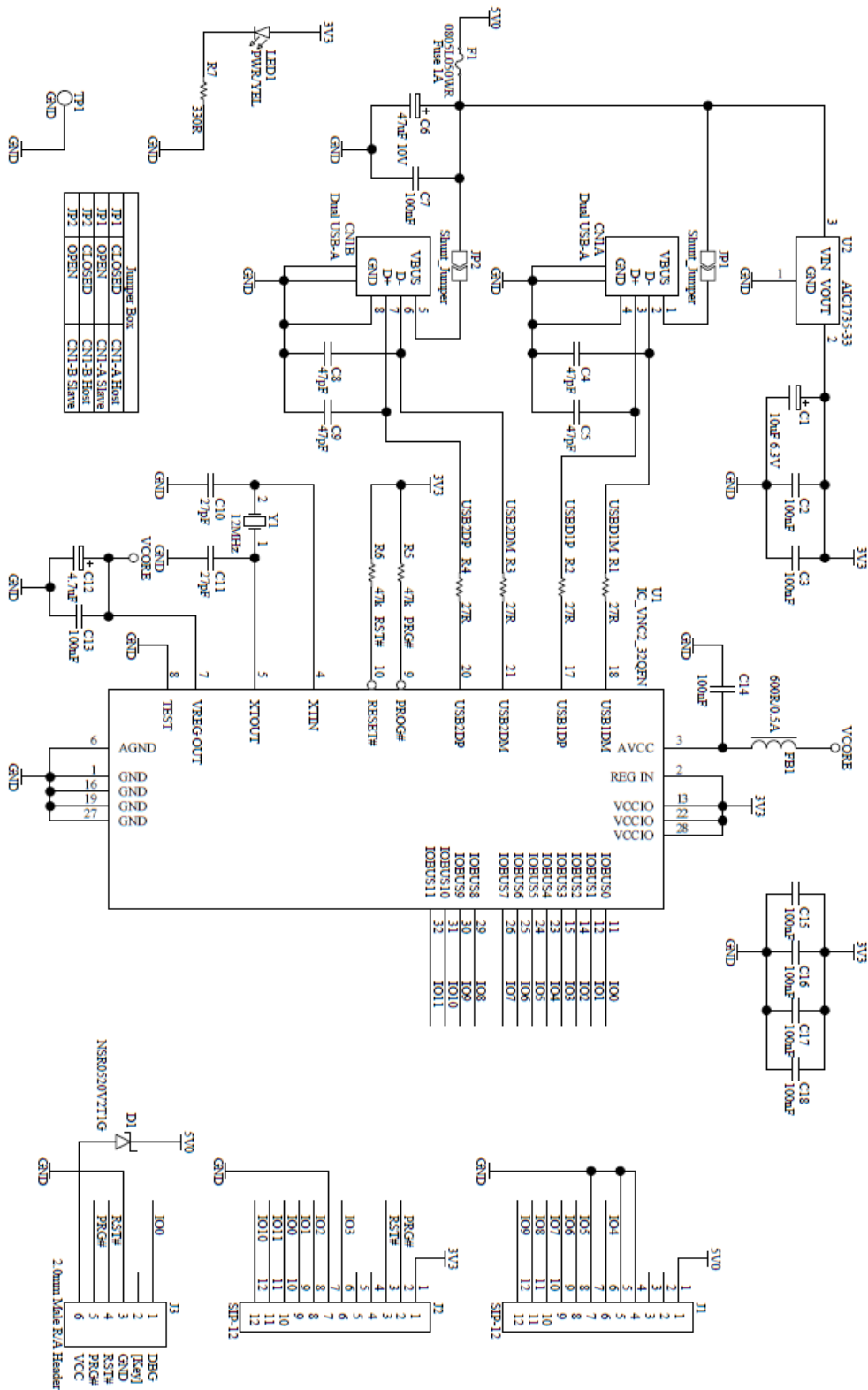


Figure 6.1 - V2DIP2-32 Schematics

7 Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place,
Centurion Business Park
Glasgow, G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com
Web Site URL <http://www.ftdichip.com>
Web Shop URL <http://www.ftdichip.com>

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)
2F, No 516, Sec. 1 NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8791 3570
Fax: +886 (0) 2 8791 3576

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com
Web Site URL <http://www.ftdichip.com>

Branch Office – Hillsboro, Oregon, USA

Future Technology Devices International Limited (USA)
7235 NW Evergreen Parkway, Suite 600
Hillsboro, OR 97123-5803
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com
Web Site URL <http://www.ftdichip.com>

Branch Office – Shanghai, China

Future Technology Devices International Limited (China)
Room 408, 317 Xianxia Road,
ChangNing District,
ShangHai, China

Tel: +86 (21) 62351596
Fax: +86(21) 62351595

E-Mail (Sales): cn.sales@ftdichip.com
E-Mail (Support): cn.support@ftdichip.com
E-Mail (General Enquiries): cn.admin1@ftdichip.com
Web Site URL <http://www.ftdichip.com>

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Application and Technical Notes

[Vinculum-II IO Cell Description](#)

[Vinculum-II Debug Interface Description](#)

[Vinculum-II IO Mux Explained](#)

[Vinculum-II PWM Example](#)

[Migrating Vinculum Designs From VNC1L to VNC2-48L1A](#)

[Vinculum-II Errata Technical Note](#)

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Appendix C – Revision History

Version 1.0 First Release

16th April 2010