NP501-00015-2v0-E

FRAM
MB85RS16

MB85RS16 is a 16K-bits FRAM LSI with serial interface (SPI), using the ferroelectric process and CMOS process technologies for forming the nonvolatile memory cells. Because FRAM is able to write high-speed even though a nonvolatile memory, it is suitable for the log management and the storage of the resume data, etc.

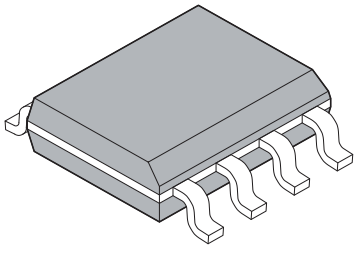
■ FEATURES

- **Bit configuration** : 2,048 words × 8 bits
- **Serial Peripheral Interface** : SPI (Serial Peripheral Interface)
  Correspondent to SPI mode 0 (0,0) and mode 3 (1,1)
- **Operating frequency** : 20 MHz (Max.)
- **High endurance** : 1 trillion Read/writes per byte
- **Data retention** : 10 years (+85°C)
- **Operating power supply voltage** : 2.7V to 3.6V
- **Low power consumption** : Operating power supply current 1.5mA (Typ@20MHz)
  Standby current 5μA (Typ)
- **Operation ambient temperature range** : -40°C to +85°C
- **Package** : 8-pin plastic SOP (FPT-8P-M02)
  8-pin plastic SON (LCC-8P-M04)
  RoHS compliant

■ ORDERING INFORMATION

Product name	Package	Shipping form	Minimum shipping quantity
MB85RS16PNF-G-JNE1	Plastic・SOP, 8-pins (FPT-8P-M02) 3.90mm×5.05mm, 1.27mm pitch	Tube	1
MB85RS16PNF-G-JNERE1	Plastic・SOP, 8-pins (FPT-8P-M02) 3.90mm×5.05mm, 1.27mm pitch	Embossed Carrier tape	1500
MB85RS16PN-G-AMERE1	Plastic・SON, 8-pins (LCC-8P-M04) 2.0mm×3.0mm, 0.5mm pitch	Embossed Carrier tape	7000

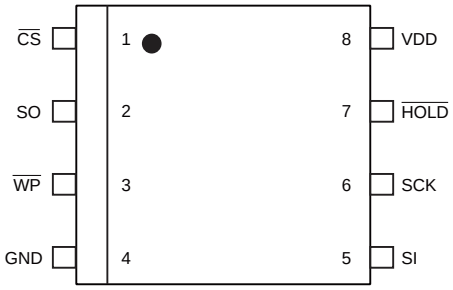
■ PACKAGE EXAMPLE OF REFERENCE



Plastic ・ SOP、8-pins
(FPT-8P-M02)

■PIN ASSIGNMENT

(TOP VIEW)



Pin No.	Pin name	Description
1	/CS	Chip Select pin This is an input pin to make chips select. When /CS is the "H" level, device is in deselect (standby) status as long as device is not write status internally, and SO becomes High-Z. Inputs from other pins are ignored at this time. When /CS is the "L" level, device is in select (active) status. /CS has to be the "L" level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin.
3	/WP	Write Protect pin This is a pin to control writing to a status register. The writing of status register is protected in related with /WP and WPEN bit of the status register.
7	/HOLD	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When /HOLD is the "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become don't care. While the hold operation, /CS has to be retained the "L" level.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	GND	Ground pin

■BLOCK DIAGRAM