IT900A MAIN FEATURES

- Low-cost Powerline Communication (PLC) modem and application solution in a single chip
- Data rates up to 500 Kbps in FCC and ARIB bands, 150 Kbps in CENELEC-A band
- Implements DCSK and DCKS Turbo Modulations
- Incorporates Yitran's high performance Data Link Layer (DLL), Network Protocol (Y-Net) and extremely robust Physical Layer (PHY)
- Zilog ZNEO microcontroller with 384KB Flash for protocol stack and application code.
- Chip Architecture options:
  - **Protocol Controller Architecture:** IT900A is accompanied by communication stack firmware
  - **Open Solution Architecture:** allows user to program application code together with the communication stack
- Full coverage even under adverse line conditions
- Fully backward compatible with IT700, IT800, and IT900 Series

APPLICATIONS

- Smart Grid Applications:
  - Automated Meter Reading (AMR)
  - Advanced Meter Management (AMM)
  - Demand Response & Real-Time pricing
- Smart Home & Energy Management:
  - Home & Building Automation
  - Home Appliance Control & Diagnostics
  - Security and Access Control
  - Environmental Control
- Commercial Applications:
  - Street Light Control
  - Vending Machine Control
  - Signage Control

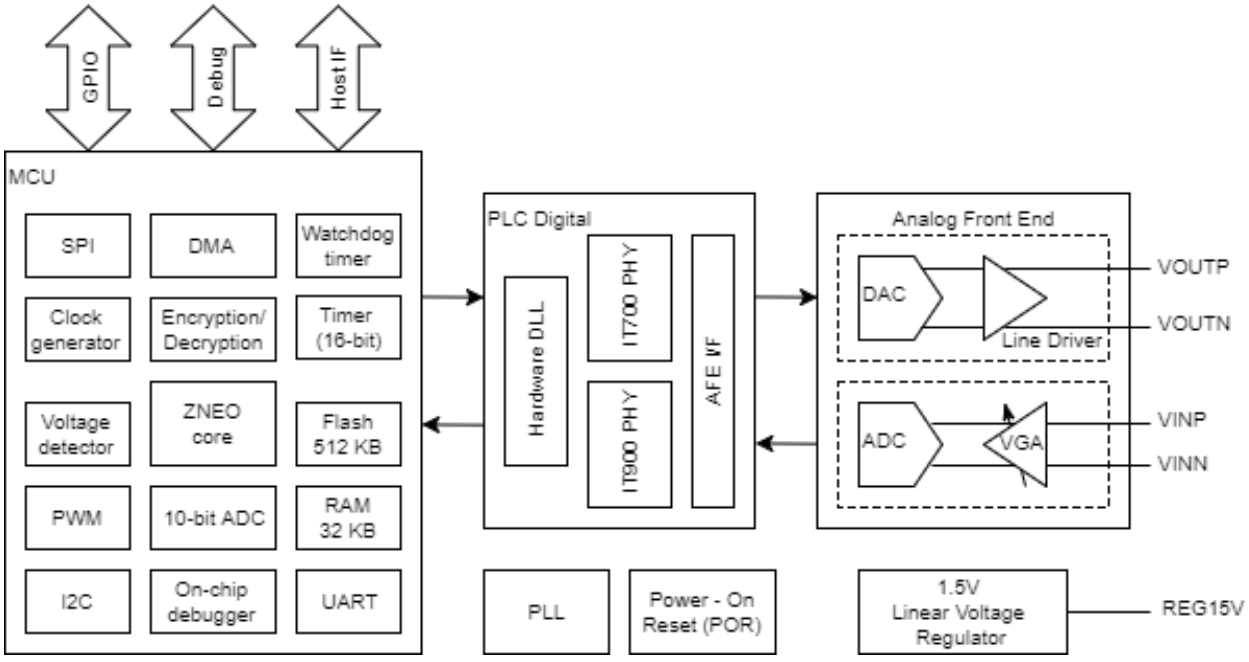

Figure 1: IT900A Block Diagram

Table of Contents

1. IT900A General Description

The IT900A is a highly integrated System-on-Chip (SoC) Powerline Communication (PLC) modem. It incorporates AFE, Yitran's extremely reliable Physical Layer (PHY) and an integrated microcontroller with Zilog ZNEO core, 384KB Flash memory, 32KB RAM and 3 eight-bit external ports can contain the protocol stack and offers the required flexibility to implement various protocols and applications. The microcontroller's UART interface provides the connection to an external Host and application controller. The I^2C interface connects an optional external EEPROM for remote firmware update.

The IT900A PLC modem core uses Yitran's patented DCSK and DCSK Turbo implementing advanced coherent spread spectrum modulation techniques for high speed and extremely robust communication with data rates up to 500 Kbps in FCC and ARIB bands, 150 Kbps in CENELEC-A band. In addition to the inherent interference immunity provided by DCSK modulation, DCSK Turbo utilizes several mechanisms for enhanced communication speed such as adaptive symbol overlapping and Decision Feedback Equalization.

The integrated AFE provides differential inputs and line driver outputs to connect via an external line filter and coupler to the power transmission lines. An integrated Phase Locked Loop Circuit allows the operation of the IT900A with a choice of different crystal oscillators. An integrated Power-On-Reset (POR) circuit eliminates the need for any external reset components and provides an autonomous, safe power-up and power-down reset to the chip. The integrated 1.5V voltage regulator allows the IT900A to operate from a single 3.3V supply.

The IT900A complies with worldwide regulations (FCC part 15, ARIB and CENELEC bands) and is an ideal solution for a variety of command and control PLC applications.

The IT900A is available in two versions:

The **Protocol Controller Architecture** version is accompanied by Yitran's Y-Net network protocol firmware. A UART interface and simple command language provide seamless connection to an external Host controller and simplify application development. In this version, no access to the microcontroller's resources is provided.

The **Open Solution Architecture** version allows utilization of the IT900A microcontroller's peripheral functions such as timers, interrupts, communication interfaces, A/D, spare memory resources and general-purpose I/Os to implement the application code, thereby eliminating the requirement for an external host controller. An Application Programming Interface (API) enables easy integration of the application code with Yitran's code.

2. Pinout and Pin Description

2.1 Pinout

The following figure shows the IT900A QFN64 lead-free package pinout:

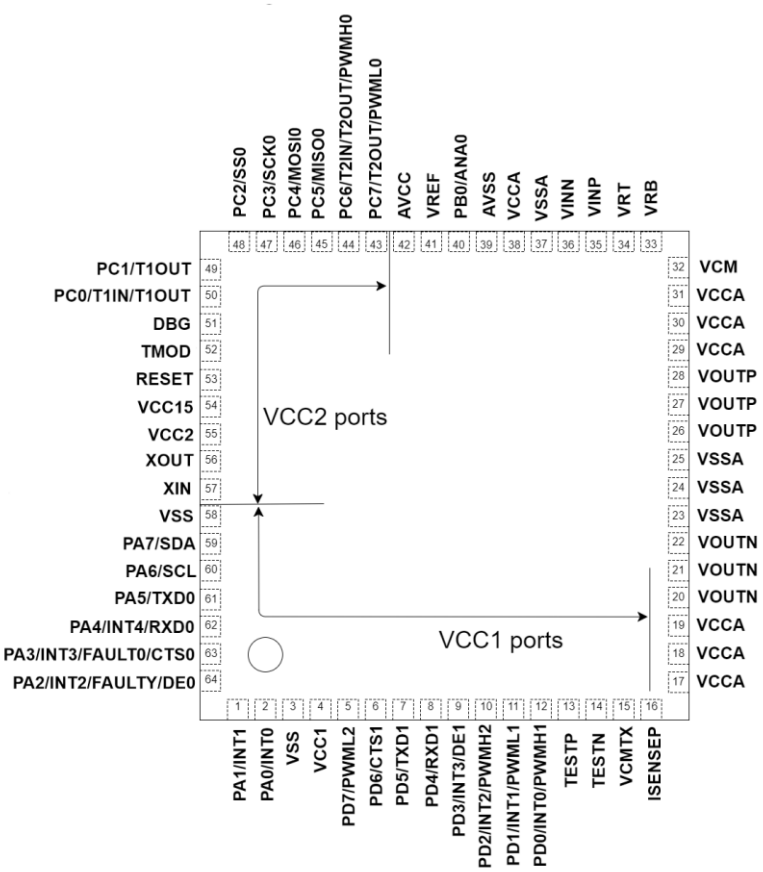

Figure 2: IT900A QFN64 Package Pinout

2.2 Pin Description

The functionality of the IT900A pins is described in Table 2. The pin type format used is xx/yy/zz and the options for the xx, yy, and zz fields are shown in the following table:

Table 1: Pin Type Syntax

xx	Description
I	Input
O	Output
IO	Input or Output

yy/zz	Description
OC	Optional Open Drain Output
PU	Optional Internal Pull-up Input
A	Analog

Table 2: IT900A Pin Description

Pin #	Pin Name Alternate Functions	Type	Description
1	**PA1** INT1	IO/PU/OC	General-purpose input/output External interrupt 1 - Input for the INT1
2	**PA0** INT0	IO/PU/OC	General-purpose input/output External interrupt 0 - Input for the INT0
3	**VSS**	Power	Digital power supply input - Apply 0 V to the VSS pin
4	**VCC1**	Power	Digital power supply input - Apply 3.3 V to the VCC1 pin
5	**PD7** PWML2	IO/PU/OC	General-purpose input/output PWM2 (Pulse Width Modulator) - PWM2 Low output
6	**PD6** CTS1	IO/PU/OC	General-purpose input/output UART1 - Input to control data transmission
7	**PD5** TXD1	IO/PU/OC	General-purpose input/output UART1 - Serial data output
8	**PD4** RXD1	IO/PU/OC	General-purpose input/output UART1 - Serial data input
9	**PD3** INT3 DE1	IO/PU/OC	General-purpose input/output External interrupt 3 - Input for the INT3 UART1 - Driver Enable: This pin allows automatic control of external RS-485 drivers. This pin is approximately the inverse of the Transmit Empty (TXE) bit in the UART1 Status 0 Register. The DE signal is used to ensure an external RS-485 driver is enabled when data is transmitted by the UART1.
10	**PD2** INT2 PWMH2	IO/PU/OC	General-purpose input/output External interrupt 2 - Input for the INT2 PWM2 (Pulse Width Modulator) - PWM2 High output
11	**PD1** INT1 PWML1	IO/PU/OC	General-purpose input/output External interrupt 1 - Input for the INT1 PWM1 (Pulse Width Modulator) – PWM1 Low output
12	**PD0** INT0 PWMH1	IO/PU/OC	General-purpose input/output External interrupt 0 - Input for the INT0 PWM1 (Pulse Width Modulator) – PWM1 High output

Pin #	Pin Name Alternate Functions	Type	Description
13	**TESTP**	I/A	Test Pin
14	**TESTN**	I/A	Test Pin
15	**VCMTX**	O	Reference voltage output pin for the analog circuit of the transmitter block. Connect to a bypass capacitor for VSSA.
16	**ISENSEP**	I/A	Input to measure output current. Connect to VOUTP through a 1-ohm resistor.
17	**VCCA**	Power	Power supply input for AFE - Apply 3.3 V to the VCCA pin
18	**VCCA**	Power	Power supply input for AFE - Apply 3.3 V to the VCCA pin
19	**VCCA**	Power	Power supply input for AFE - Apply 3.3 V to the VCCA pin
20	**VOUTN**	O/A	TX Signal - Output pin for differential transmission signal - N
21	**VOUTN**	O/A	TX Signal - Output pin for differential transmission signal - N
22	**VOUTN**	O/A	TX Signal - Output pin for differential transmission signal - N
23	**VSSA**	Power	Power supply input for AFE - Apply 0 V to the VSSA pin
24	**VSSA**	Power	Power supply input for AFE - Apply 0 V to the VSSA pin
25	**VSSA**	Power	Power supply input for AFE - Apply 0 V to the VSSA pin
26	**VOUTP**	O/A	TX Signal - Output pin for differential transmission signal - P
27	**VOUTP**	O/A	TX Signal - Output pin for differential transmission signal - P
28	**VOUTP**	O/A	TX Signal - Output pin for differential transmission signal - P
29	**VCCA**	Power	Power supply input for AFE - Apply 3.3 V to the VCCA pin
30	**VCCA**	Power	Power supply input for AFE - Apply 3.3 V to the VCCA pin
31	**VCCA**	Power	Power supply input for AFE - Apply 3.3 V to the VCCA pin
32	**VCM**	O/A	Reference voltage output pin for the analog circuit of receiver block. Connect to a bypass capacitor for VSSA.
33	**VRB**	O/A	Reference voltage output pins for ADC of PLC block. Connect to a bypass capacitor for VSSA.
34	**VRT**	O/A	Reference voltage output pins for ADC of PLC block. Connect to a bypass capacitor for VSSA.
35	**VINP**	I/A	Rx Signal - Input pin for differential reception signal - P
36	**VINN**	I/A	Rx Signal - Input pin for differential reception signal - N
37	**VSSA**	Power	Power supply input for AFE - Apply 0 V to the VSSA pin
38	**VCCA**	Power	Power supply input for AFE - Apply 3.3 V to the VCCA pin
39	**AVSS**	Power	Power Supply input for MCU ADC - Apply 0 V to the AVSS pin
40	**ANA0**	I/A	Analog input for MCU ADC
41	**VREF**	IO	Reference Voltage input or Internal Reference output for MCU ADC. Connect to a 100nF capacitor for AVSS if internal reference voltage is selected.
42	**AVCC**	Power	Power Supply input for MCU ADC - Apply 3.3 V to the AVCC pin
43	**PC7** T2OUT PWML0	IO/PU/OC	General-purpose input/output Timer2 - Output for Timer2 PWM0 (Pulse Width Modulator) – PWM0 Low output
44	**PC6** T2IN T2OUT PWMH0	IO/PU/OC	General-purpose input/output Timer2 - Input for Timer2 Timer2 - Output for Timer2 PWM0 (Pulse Width Modulator) – PWM0 High output

Pin #	Pin Name Alternate Functions	Type	Description
45	**PC5** MISO0	IO/PU/OC	General-purpose input/output SPI0 - Master-In/Slave-Out: This pin is the data input to the SPI master device and the data output from the SPI slave device.
46	**PC4** MOSI0	IO/PU/OC	General-purpose input/output SPI0 – Master-Out/Slave-In: This pin is the data output from the SPI master device and the data input to the SPI slave device.
47	**PC3** SCK0	IO/PU/OC	General-purpose input/output SPI0 -SPI serial clock: The SPI master supplies this pin. If the ZNEO is the SPI master, this pin is an output. If the ZNEO is the SPI slave, this pin is an input.
48	**PC2** SS0	IO/PU/OC	General-purpose input/output SPI0 - Slave select: This pin is an output or an input. If ZNEO is the SPI master, this pin is configured as the slave select output. If ZNEO is the SPI slave, this pin is an input slave select.
49	**PC1** T1OUT	IO/PU/OC	General-purpose input/output Timer1 - Output for timer 1
50	**PC0** T1IN T1OUT	IO/PU/OC	General-purpose input/output Timer1 - Input for timer 1 Timer1 - Output for timer 1
51	**DBG**	IO/OC	Debug: This pin is the control and data input/output to and from the OCD. For operation of the OCD, all power pins (VCC and AVCC) must be supplied with power and all ground pins (VSS and AVSS) must be grounded. This pin is open-drain and must have an external pull-up resistor to ensure proper operation.
52	**TMOD**	I	Test mode: This pin is Not Connected.
53	**RESET**	I/PU	Reset: This pin is Active Low.
54	**VCC15**	O	Regulator output pin (1.5 V) for the digital circuit of PLC block. Connect only to a bypass capacitor for VSS. Do not use this pin to provide power to other circuits.
55	**VCC2**	Power	Digital power supply input - Apply 3.3 V to the VCC2 pin
56	**XOUT**	O	Main clock - Output for the main clock oscillation circuit. Connect crystal oscillator between pins XIN and XOUT
57	**XIN**	I	Main clock – Input for the main clock oscillation circuit. Connect crystal oscillator between pins XIN and XOUT.
58	**VSS**	Power	Digital power supply input - Apply 0 V to the VSS pin
59	**PA7** SDA	IO/PU/OC	General-purpose input/output I²C - Transmit/receive data I/O for I²C
60	**PA6** SCL	IO/PU/OC	General-purpose input/output I²C - Transmit/receive clock I/O for I²C
61	**PA5** TXD0	IO/PU/OC	General-purpose input/output UART 0 - Serial data output

Pin #	Pin Name Alternate Functions	Type	Description
62	**PA4** INT4 RXD0	IO/PU/OC	General-purpose input/output External interrupt 4 - Input for the INT4 UART0 - Serial data input
63	**PA3** INT3 FAULT0 CTS0	IO/PU/OC	General-purpose input/output External interrupt 3 - Input for the INT3 PWM0 (Pulse Width Modulator) – PWM Fault condition input 0 - active Low UART0 - Input to control data transmission
64	**PA2** INT2 FAULT1 DE0	IO/PU/OC	General-purpose input/output External interrupt 2 - Input for the INT2 PWM0 (Pulse Width Modulator) – PWM Fault condition input 1 - active Low UART0 - Driver Enable: This pin allows automatic control of external RS-485 drivers. This pin is approximately the inverse of the Transmit Empty (TXE) bit in the UART0 Status 0 Register. The DE signal is used to ensure an external RS-485 driver is enabled when data is transmitted by the UART0.

3. PHY Specifications and Operating Modes

The following table details IT900A PHY specifications and operating modes:

Table 3: PHY Specification and Operating Modes

Parameter		Value
Dynamic Range		100 dB
Narrowband Interference rejection		−60dB
AWGN Interference rejection		−7dB
Maximum Data Rate	FCC and ARIB	120kHz to 400kHz • Up to 500 Kbps in DCSK Turbo Modulation • Up to 7.5 kbps in DCSK Modulation
	CENELEC A	A Band: 9kHz to 95 kHz • Up to 150 Kbps in DCSK Turbo Modulation • Up to 2.5 kbps in DCSK Modulation
	CENELEC B	B Band: 95 kHz to 125 kHz • Up to 50 Kbps in DCSK Turbo Modulation • Up to 2.5 kbps in DCSK Modulation
Output Tx Power	FCC	1.1 dBm @ BW=1kHz
	ARIB	-3 dBm @ BW=1kHz
	CENELEC A	5.6 dBm @ BW=1kHz
	CENELEC B	9.5 dBm @ BW=1kHz

Each signal band requires suitable configuration of the PLC modem, adjusting the input filter to a signal band and output amplitude, setting.

Refer to the following standards about the regulation of a signal level outside the band.
- U.S.: FCC standard, part 15
- Europe: CENELEC standard, EN 50065-1
- Japan: ARIB, STD-T84

4. Analog Front-End (AFE)

The IT900A interfaces to the power line medium via an integrated Analog Front End (AFE). The AFE consists of the following main building blocks as shown in Figure 3:

1. Digital-to-Analog Converter (DAC) that converts the digital transmit-data from the PHY into an analog waveform to be transmitted over the power line.
2. Line Driver to amplify the analog signal provided by the DAC before it is coupled onto the power line.
3. Variable Gain Amplifier (VGA) to amplify the analog receive-data waveform coming from the power line coupler, thereby better utilizing the full dynamic range of the ADC.
4. Analog-to-Digital Converter (ADC) that converts the analog receive-data waveform, which is amplified by the VGA, into digital data that are then sent to the PHY.
5. Digital interface to and from the PHY transmitter and receiver blocks.

Analog front end (AFE) is the circuit located between PLC PHY and a power line. There are the following two signal paths in the AFE.

- Transmitting path: Consists of a DAC driven by the internal port, a low-pass filter (LPF), a differential Line Driver amplifier and a line coupling circuit which drives the power line.
- Receiving path: Consists of a line coupling circuit, an input filter, a differential VGA amplifier, a LPF) and an ADC. The line coupling circuit is common to both transmission and reception.

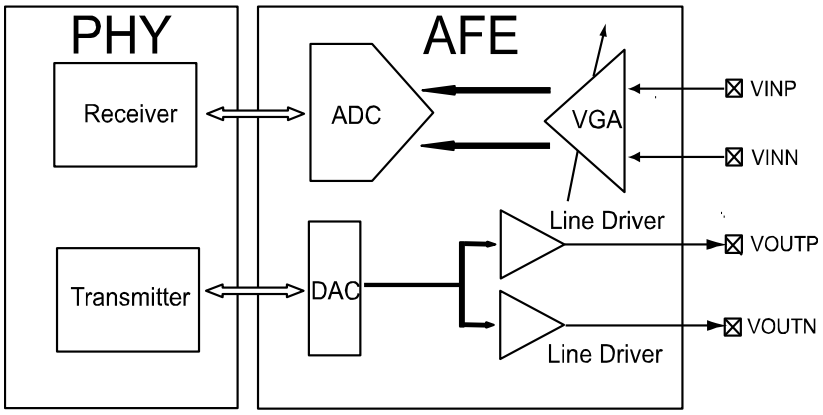

Figure 3: AFE Block Diagram

5. Enhanced ZNEO Microcontroller

The IT900A features an integrated Zilog ZNEO microcontroller, running at a system clock frequency of 26.33MHz with 384KB of Flash program memory and 32KB RAM data memory.

Table 4: ZNEO Specifications

Item	Function	Description
CPU	Central processing unit	ZNEO Series core • Number of 32-bit registers: 16 • Number of basic instructions: 65 • Minimum instruction execution time: 38 ns (f = 26.33 MHz, VCC1 = VCC2 = 3.0 to 3.6 V)
Memory	RAM, data flash	
Clock	Clock generator	Single 15.36MHz external crystal with on-board PLL to generate system clocks: CPU core: 26.33MHz PLC core: 46.08MHz
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 56 selectable pull-up resistors, selectable open drain (32 used for PLC modem connection)
Interrupts		• Interrupt vectors: 32 (3 used for PLC modem connection) • External interrupt inputs: 8 (3 used for PLC modem connection) • Interrupt priority levels: 3 + disabled
Watchdog Timer		• 16-bit timer: 1 (with prescaler) • Automatic reset start function selectable
DMA	DMAC	• Independent channels: 4 • Trigger sources: 14 • Transfer modes: 2 (direct transfer, linked list transfer)
Timers	Timer	• 16-bit timer: 5 (1 used for PLC modem connection) • Modes: One-shot, Continuous, Counter, PWM, Capture, Compare and Gated mode
Serial Interface	LIN-UART	• Channels: 2 • Configurable digital noise filter
	Enhanced SPI	• Channels: 2 (1 used for PLC modem connection) • SPI and Inter IC Sound (I²S) modes • Error detection
	I²C-bus interface	• Channels: 1
A/D Converter		• Channels: 1 • Resolution: 10-bit, including sample and hold function • Conversion time: 13 ADC clock cycles
CRC Calculator		CRC-CCITT (X16 + X12 + X5 + 1), CRC-16 (X16 + X15 + X2 + 1) compliant
Encryption	AES	AES Encryption (Key length: 128 bits)
Flash Memory		• Erase/write power supply voltage: 2.7 to 3.6 V • Erase/write cycles: 100,000 times • Program security: ROM code protect

6. Y-Net Protocol

6.1 YNET Protocol General Description

The IT900A is accompanied by Yitran's Y-Net protocol firmware. The Y-Net protocol stack firmware implements Media Access Control (MAC) and Network Layer (NL), which are layers 2 and 3 of the seven-layer OSI model highlighted in grey the following figure.

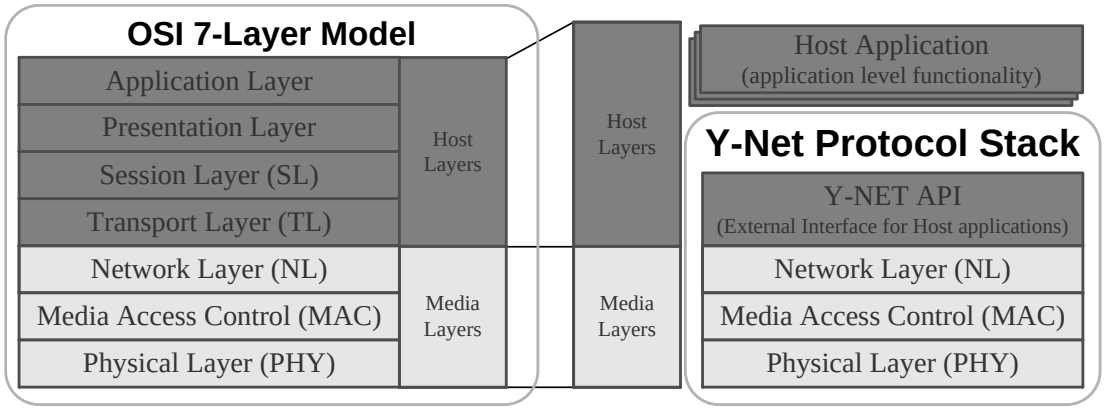

Figure 4: YNET Protocol Stack

The Y-Net protocol stack consists of the following:

- **Physical (PHY) layer** - The PHY consisting of the physical interface to the power line media.
- **Media Access Control (MAC) layer** - The MAC layer implements a highly efficient channel access management function, which enables the channel tobe occupied by only a single node at any given time while providing adequate Quality of Service (QoS) among nodes and maintaining high overall network throughput
- **Network layer (NL)** - The NL transparently creates and maintains a tree-type topology network and releases the upper layer from the responsibility of handling the constantly changing conditions of the power line media.
  The logical network consists of a Network Coordinator (NC) node responsible for network formation activities. The NC is expected to remain online most of the time. All other nodes in the logical network are remote stations (RS).
  An RS may serve as a router to route packets to or from the NC and may also implement remote application functionality.

6.2 YNET Protocol Main Features

LAYER 1 (PHY)

- Patented DCSK and DCSK Turbo implementing advanced coherent spread spectrum modulation techniques
- High immunity to signal fading, noise, impedance modulation and phase/ frequency distortions
- High in-phase and cross-phase reliability
- Forward short-block soft decoding error correction mechanism and CRC-16
- Complies with FCC, ARIB and EN50065-1-CENELEC regulations
- FCC and ARIB bands bit rate up to 500 Kbps
- CENELEC band bit rate up to 150 Kbps

LAYER 2 (MAC)

- Up to 1023 logical networks and 2047 nodes per network
- Acknowledged and Unacknowledged data transmission services
- Re-transmission mechanism
- Automatic rate control
- Adaptive Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) channel access
- Fragmentation and re-assembly to support full Ethernet packet transmission

LAYER 3 (NETWORK)

- Supports 1000 different, overlapping networks
- Supports 2000 nodes in each network
- Master-Slave and Peer-to-Peer Network Configurations
- Plug & Play Network Setup
- Automatic logical network creation
- Automatic node address allocation
- Automatic and adaptive Routing Service (Tree topology)
- Network Parameter Recovery
- Failure Detection
- Full security Suite including AES 128-bit encryption with 32-bit authentication

7. Host Interface

The IT900A Protocol Controller Architecture version is accompanied by Yitran‟s Y-Net protocol stack pre-programmed.
In this mode, the device operates as a PLC modem chip with interface to an external host application. The external host application is required to implement the application layer functionality. The host controller connects to the IT900A through a full-duplex UART physical interface. A command set provides the logical interface from the host application to the IT900A network layer.

Figure 5 shows the typical schematic connections for the IT900A Protocol Controller Architecture.

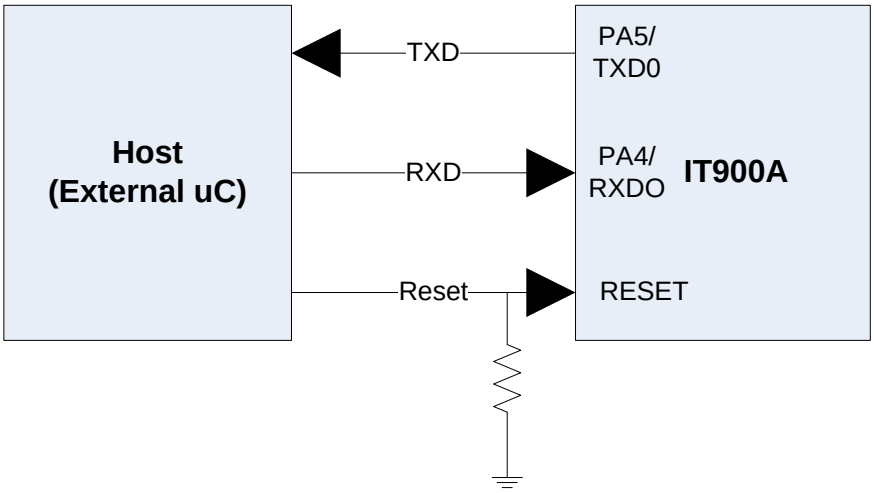

Figure 5: Host Interface

8. Electrical Characteristics

8.1 Absolute Maximum Operating Conditions

These are stress ratings only: functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Stresses beyond those listed under "Absolute Maximum Operating Conditions" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5: Absolute Maximum Operating Conditions

Parameter		Min	Max	Unit
Supply Voltage	VCC1	-0.3	4.3	V
	VCC2	-0.3	VCC1+0.1 (*)	
	VCCA	-0.3	4.3	
Analog Supply Voltage	AVCC	-0.3	4.3	V
	VREF	-0.3	VCC1+0.1 (*)	
Input Voltage				V
DBG, TMOD, CNVSS, PA0 to PA7, XIN, PD0 to PD7	VI	-0.3	VCC1+0.3 (*)	
UROM_EN, PC0 to PC7		-0.3	VCC2+0.3 (*)	
VINP, VINN, TESTP, TESTN, OC_EN		-0.3	VCCA+0.3 (*)	
Output Voltage				V
DBG, PA0-PA7, XOUT, PD0-PD7	VO	-0.3	VCC1+0.3 (*)	
TS, PC0 to PC7		-0.3	VCC2+0.3 (*)	
VOUTP, VOUTN, EXTLDP, EXTLDN, VCM, VCMTX, VRT, VRB, TESTP, TESTN, OC		-0.3	VCCA+0.3 (*)	
VCC15		-0.3	1.8	

(*) Maximum value is 4.3V

8.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

VCC1=VCC2=3.0 to 3.6V at Topr = -40ºC to 85ºC unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply Voltage [1]	VCC1	3.0		3.6	V	VCC1=VCC2=VCCA
	VCC2		VCC1			VCC1=VCC2=VCCA
	VCCA		VCC1			VCC1=VCC2=VCCA
Analog Supply Voltage	AVCC		VCC1		V	
Supply Voltage	VSS		0		V	
	VSSA		0			
Analog Supply Voltage	AVSS		0		V	
Supply voltage rise gradient	Tvccg	5		50K	V/s	VCC1=VCC2=VCCA
High Input Voltage DBG, TMOD, PA0 to PA7, XIN, PD0 to PD7, PB0 to PB7, PC0 to PC7	VIH	2			V	
Low Input Voltage DBG, TMOD, PA0 to PA7, XIN, PD0 to PD7 PB0 to PB7, PC0 to PC7	VIL			0.8	V	
Operating Temperature	Topr	-40		85	ºC	

Recommended operating conditions (1/3)

VCC1=VCC2=3.0 to 3.6V at Topr = -40ºC to 85ºC unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal Oscillator Frequency	f(XIN)		15.46		MHz	
PLL clock Oscillation Frequency	f(PLL)		26.33		MHz	
PLL Frequency Synthesizer Stabilization Time	fsu(PLL)			3	ms	

Recommended operating conditions (2/3)

VCC1=VCC2=3.0to 3.6V at Topr = -40ºC to 85ºC unless otherwise specified
The ripple voltage must not exceed Vr(VCC1) or dVr(VCC1/)dt

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Allowable Ripple Voltage	Vr(VCC1)			0.3	Vpp	

Recommended operating conditions (3/3)

[1] VCC1, VCC2, VCCA and AVCC supplied from same source

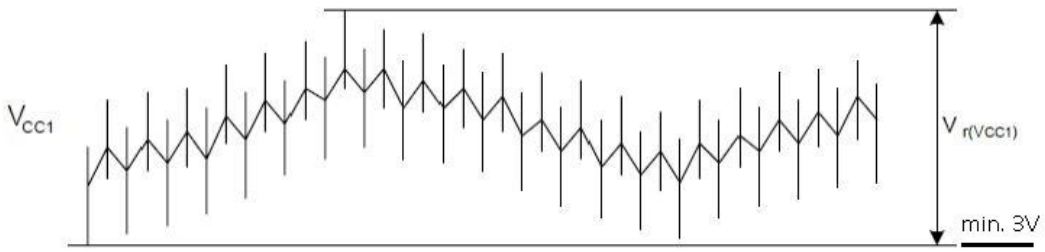

Figure 6: Ripple Waveform

9. Application Circuit

Figure 7 below shows a typical schematic connection for the IT900A application circuit (the EEPROM is optional). Please refer to IT900A PIM9A Reference Design for more details.

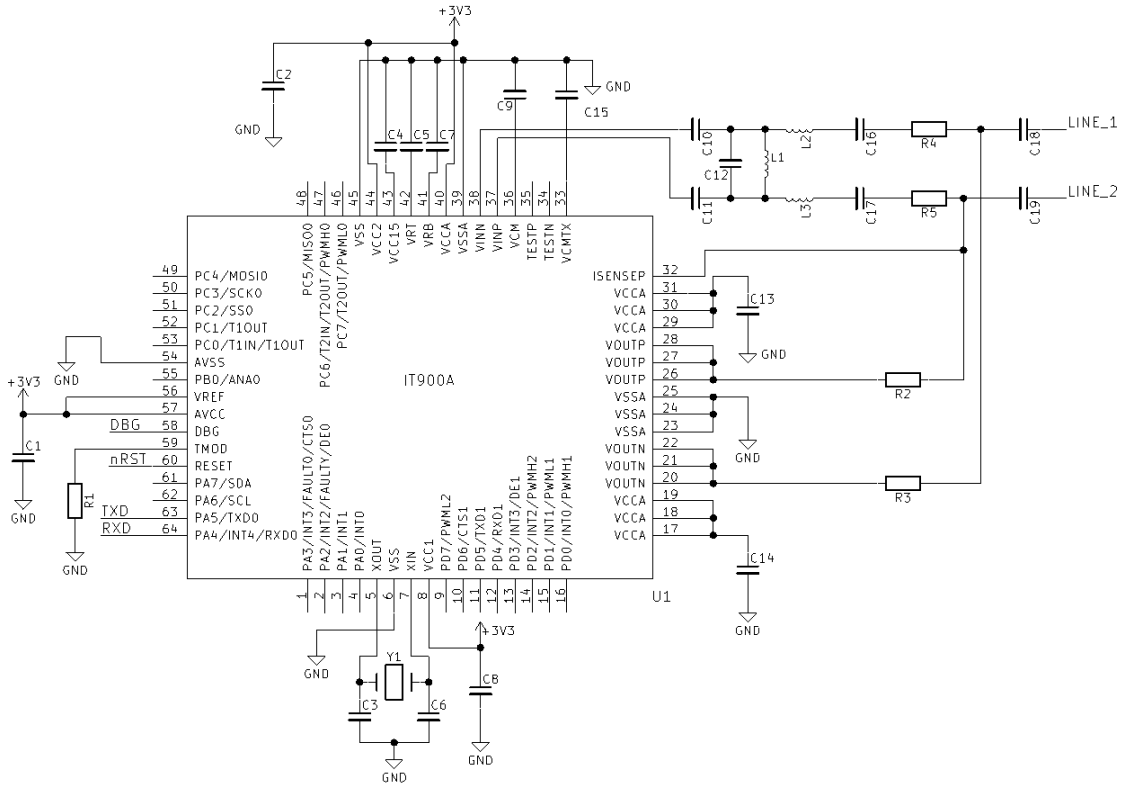

Figure 7: Typical Application Diagram

The IT900A Line Coupler "connects" the PLC modem to the power line. The coupler provides the required insulation between high and low voltage sections and converts a balanced output of the modem to an unbalanced power line. Figure 8 below shows a recommended line coupler circuit.

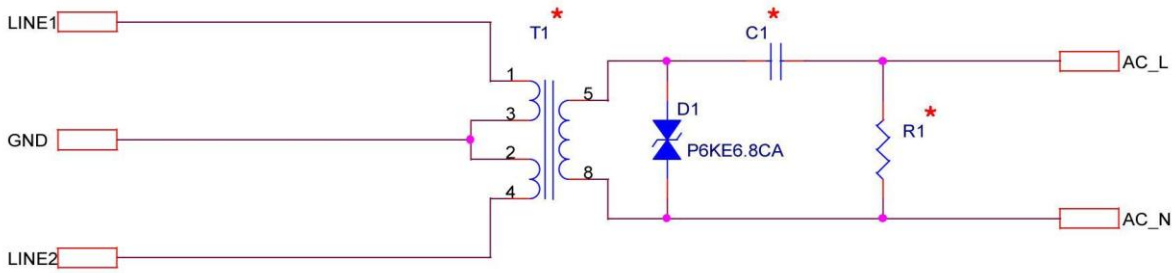

Figure 8: Line Coupler Recommended Circuit

10. Mechanical Dimensions

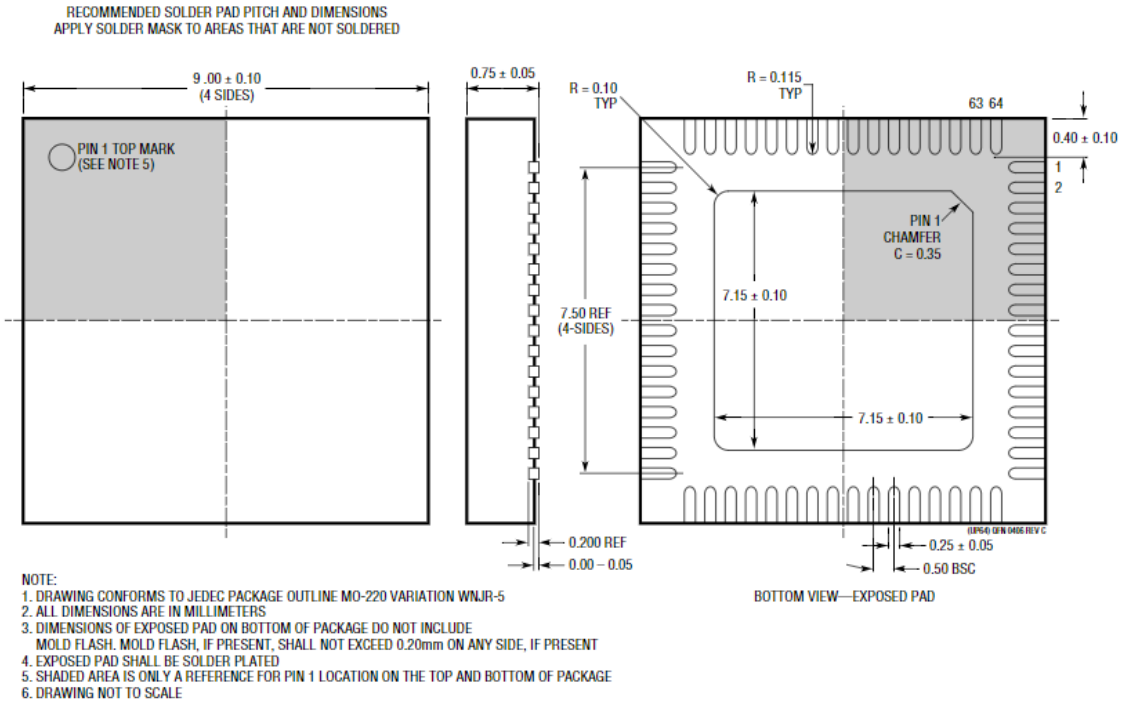

Figure 9: Mechanical Dimensions

11. Ordering Information

The IT900A part naming convention for ordering parts is shown below:

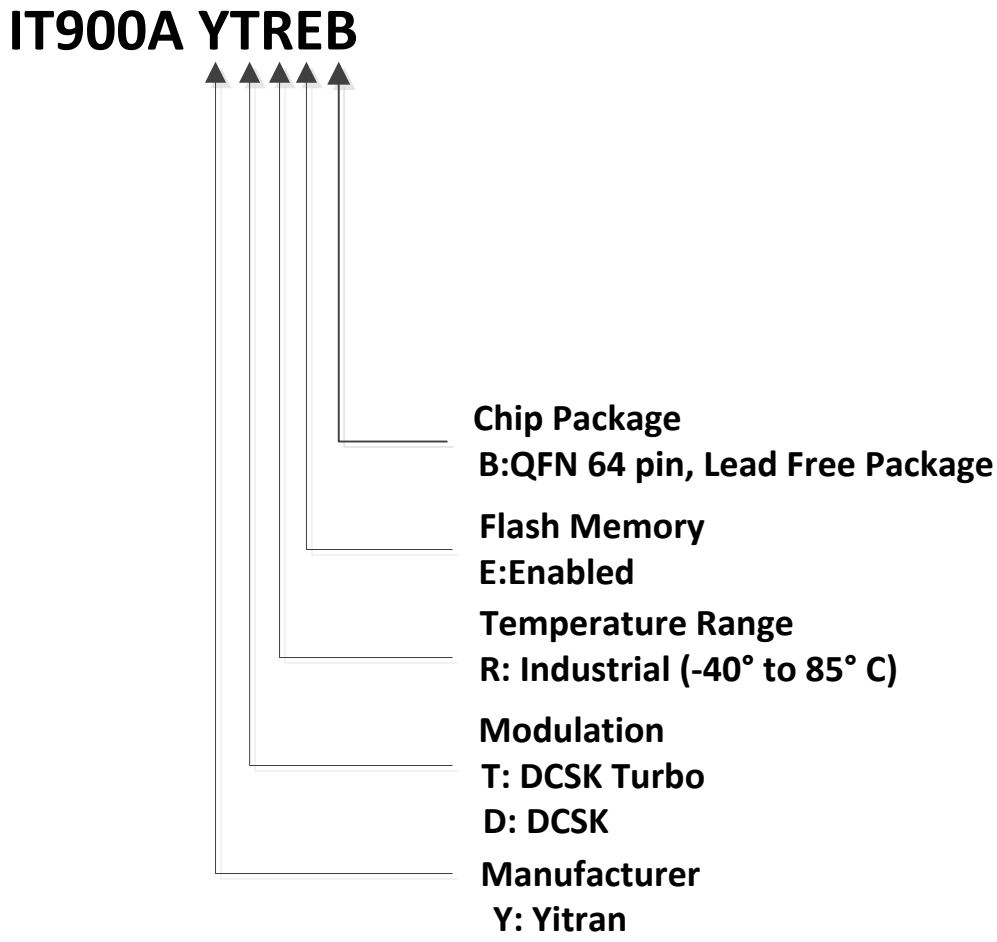

Figure 10: Ordering Information

Document Control

Rev	Date	Description
1.0	June 24, 2020	Initial Release
1.1		
1.2		

Important Notice

All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability. Yitran Technologies Ltd. ("Yitran") reserves the right to make changes to its products, except for encryption and authentication algorithms, or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete.

Yitran warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with Yitran's standard warranty. Testing and other quality control techniques are utilized to the extent Yitran deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications"). Yitran's PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE–SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF Yitran's PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, the customer, to minimize inherent or procedural hazards, must provide adequate design and operating safeguards.

Yitran assumes no liability for applications assistance or customer product design. Yitran does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of Yitran covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. Yitran's publication of information regarding any third party's products or services does not constitute Yitran's approval, warranty or endorsement thereof.

Yitran Tecnologies Ltd.
8 HaGoren St.
Omer 8496500
ISRAEL

T +972 8 958 0282
F +972 8 958 0281
yitran@yitran.com

