

RoHS Compliant

8GB DDR4 SDRAM UDIMM **Halogen free**

Product Specifications

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Version 0.3



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General Description

Apacer **78.C1GMM.AF50B** is a 1024M x 64 DDR4 SDRAM (Synchronous DRAM) DIMM. This high-density memory module consists of 8 pieces 1024M x 8 bits with 4 banks DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 288-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
78.C1GMM.AF50B	19.2 GB/sec	2400 Mbps	1200 MHz	CL17

Density	Organization	Component	Rank
8GB	1024M x 64	1024M x8*8	1

Key Parameters

MT/s	DDR4-1866	DDR4-2133	DDR4-2400	Unit
Grade	-CL13	-CL15	-CL17	
tCK (min)	1.07	0.93	0.83	ns
CAS latency	13	15	17	tCK
tRCD (min)	13.92	14.06	14.16	ns
tRP (min)	13.92	14.06	14.16	ns
tRAS (min)	34	33	32	ns
tRC (min)	47.92	47.05	46.16	ns
CL-tRCD-tRP	13-13-13	15-15-15	17-17-17	tCK

Specifications:

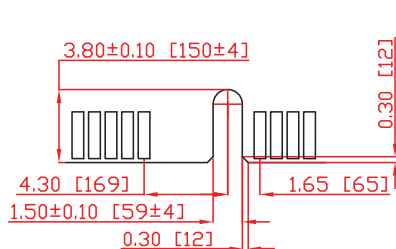
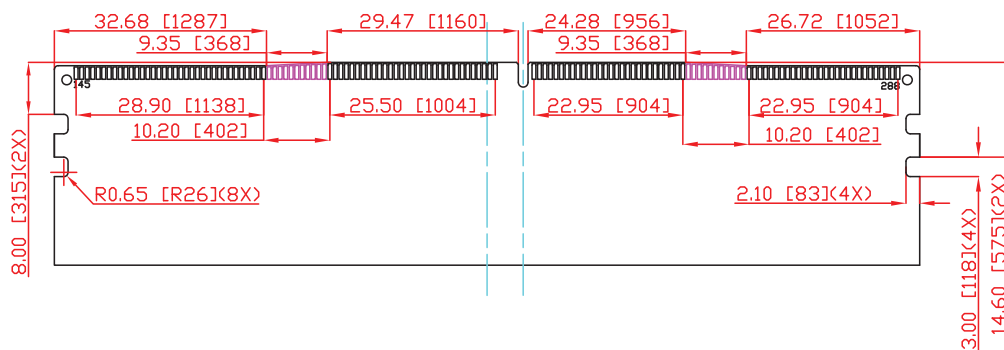
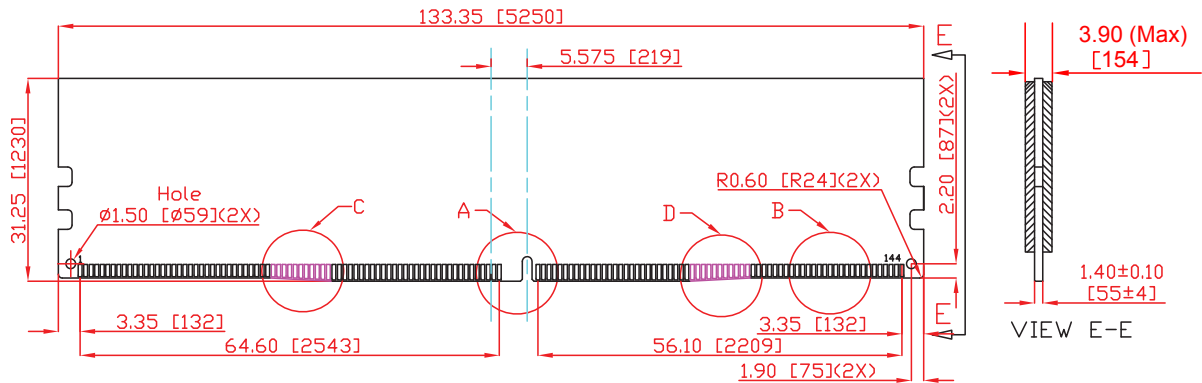
- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 1024 words x 64 bits, 1 rank
- ◆ Integrating 8 pieces of 8G bits DDR4 SDRAM sealed FBGA
- ◆ Package: 288-pin socket type dual in-line memory module (DIMM)
- ◆ PCB: height 31.25 mm, lead pitch 0.85 mm (pin),
- ◆ Serial Presence Detect (SPD)
- ◆ Power Supply: VDD=1.2V (1.14V to 1.26V)
- ◆ VDDQ = 1.2V (1.14V to 1.26V)
- ◆ VPP = 2.5V (2.375V to 2.75V)
- ◆ VDDSPD = 2.2V to 3.6V
- ◆ 16 internal banks (4 Bank Groups)
- ◆ CAS Latency (CL): 13, 14, 15, 16, 17
- ◆ CAS Write Latency (CWL): 12, 16
- ◆ Average refresh period
 - 7.8us at $0^{\circ}\text{C} \leq \text{TC} \leq 85^{\circ}\text{C}$
 - 3.9us at $85^{\circ}\text{C} \leq \text{TC} \leq 95^{\circ}\text{C}$
- ◆ Lead-free (RoHS compliant)
- ◆ Halogen free

Features:

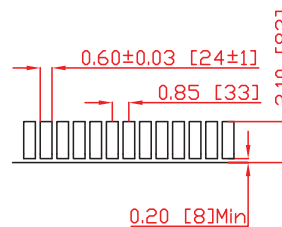
- ◆ Functionality and operations comply with the DDR4 SDRAM datasheet
- ◆ Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- ◆ Bi-Directional Differential Data Strobe
- ◆ 8 bit pre-fetch
- ◆ Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- ◆ Per DRAM Addressability is supported
- ◆ Internal Vref DQ level generation is available
- ◆ Write CRC is supported at all speed grades
- ◆ DBI (Data Bus Inversion) is supported(x8)
- ◆ CA parity (Command/Address Parity) mode is supported

Mechanical Drawing

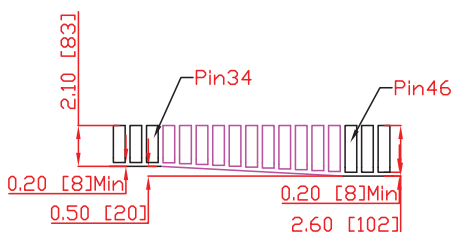
Unit: mm



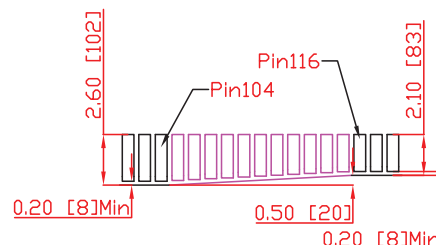
Detail A



Detail B



Detail C



Detail D

(All dimensions are in millimeters with ± 0.15 mm tolerance unless specified otherwise.)

Global Presence

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