

RoHS Compliant

16GB DDR4 SDRAM UDIMM **Halogen free**

Product Specifications

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Version 0.2



Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan

Tel: +886-2-2267-8000 Fax: +886-2-2267-2261

www.apacer.com

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General Description

Apacer **78.D1GMM.4010B** is a 2048M x 64 DDR4 SDRAM (Synchronous DRAM) DIMM. This high-density memory module consists of 16 pieces 1024M x 8 bits with 4 banks DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 288-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

| Part Number | Bandwidth | Speed Grade | Max Frequency | CAS Latency |
|----------------|-------------|-------------|---------------|-------------|
| 78.D1GMM.4010B | 19.2 GB/sec | 2400 Mbps | 1200 MHz | CL17 |

| Density | Organization | Component | Rank |
|---------|--------------|-------------|------|
| 16GB | 2048M x 64 | 1024M x8*16 | 2 |

Key Parameters

| MT/s | DDR4-1866 | DDR4-2133 | DDR4-2400 | Unit |
|-------------|-----------|-----------|-----------|------|
| Grade | -CL13 | -CL15 | -CL17 | |
| tCK (min) | 1.07 | 0.93 | 0.83 | ns |
| CAS latency | 13 | 15 | 17 | tCK |
| tRCD (min) | 13.92 | 14.06 | 14.16 | ns |
| tRP (min) | 13.92 | 14.06 | 14.16 | ns |
| tRAS (min) | 34 | 33 | 32 | ns |
| tRC (min) | 47.92 | 47.05 | 46.16 | ns |
| CL-tRCD-tRP | 13-13-13 | 15-15-15 | 17-17-17 | tCK |

Specifications:

- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 2048 words x 64 bits, 2 ranks
- ◆ Integrating 16 pieces of 8G bits DDR4 SDRAM sealed FBGA
- ◆ Package: 288-pin socket type dual in-line memory module (DIMM)
- ◆ PCB: height 31.25 mm, lead pitch 0.85 mm (pin),
- ◆ Serial Presence Detect (SPD)
- ◆ Power Supply: VDD=1.2V (1.14V to 1.26V)
- ◆ VDDQ = 1.2V (1.14V to 1.26V)
- ◆ VPP = 2.5V (2.375V to 2.75V)
- ◆ VDDSPD = 2.2V to 3.6V
- ◆ 16 internal banks (4 Bank Groups)
- ◆ CAS Latency (CL): 13, 14, 15, 16, 17
- ◆ CAS Write Latency (CWL): 12, 16
- ◆ Average refresh period
 - 7.8us at $0^{\circ}\text{C} \leq \text{TC} \leq 85^{\circ}\text{C}$
 - 3.9us at $85^{\circ}\text{C} \leq \text{TC} \leq 95^{\circ}\text{C}$
- ◆ Lead-free (RoHS compliant)
- ◆ Halogen free

Features:

- ◆ Functionality and operations comply with the DDR4 SDRAM datasheet
- ◆ Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- ◆ Bi-Directional Differential Data Strobe
- ◆ 8 bit pre-fetch
- ◆ Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- ◆ Per DRAM Addressability is supported
- ◆ Internal Vref DQ level generation is available
- ◆ Write CRC is supported at all speed grades
- ◆ DBI (Data Bus Inversion) is supported(x8)
- ◆ CA parity (Command/Address Parity) mode is supported

Pin Assignments

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|---|---------|----------|---------|---|---------|---------------|
| 1 | 12 V, NC | 145 | 12 V, NC | 74 | CK0_t | 218 | CK1_t |
| 2 | VSS | 146 | VREFCA | 75 | CK0_c | 219 | CK1_c |
| 3 | DQ4 | 147 | VSS | 76 | VDD | 220 | VDD |
| 4 | VSS | 148 | DQ5 | 77 | VTT | 221 | VTT |
| 5 | DQ0 | 149 | VSS | 78 | EVENT_n | 222 | PARITY |
| 6 | VSS | 150 | DQ1 | 79 | A0 | 223 | VDD |
| 7 | TDQS9_t, DQS9_t, DM0_n, DBI0_n, NC | 151 | VSS | 80 | VDD | 224 | BA1 |
| 8 | TDQS9_c, DQS9_c, NC | 152 | DQS0_c | 81 | BA0 | 225 | A10/AP |
| 9 | VSS | 153 | DQS0_t | 82 | RAS_n/A16 | 226 | VDD |
| 10 | DQ6 | 154 | VSS | 83 | VDD | 227 | RFU |
| 11 | VSS | 155 | DQ7 | 84 | CS0_n | 228 | WE_n/A14 |
| 12 | DQ2 | 156 | VSS | 85 | VDD | 229 | VDD |
| 13 | VSS | 157 | DQ3 | 86 | CAS_n/A15 | 230 | NC, SAVE_n |
| 14 | DQ12 | 158 | VSS | 87 | ODT0 | 231 | VDD |
| 15 | VSS | 159 | DQ13 | 88 | VDD | 232 | A13 |
| 16 | DQ8 | 160 | VSS | 89 | CS1_n, NC | 233 | VDD |
| 17 | VSS | 161 | DQ9 | 90 | VDD | 234 | NC, A17 |
| 18 | TDQS10_t, DQS10_t, DM1_n, DBI1_n, NC | 162 | VSS | 91 | ODT1, NC | 235 | NC, C2 |
| 19 | TDQS10_c, DQS10_c, NC | 163 | DQS1_c | 92 | VDD | 236 | VDD |
| 20 | VSS | 164 | DQS1_t | 93 | C0, CS2_n, NC | 237 | NC, CS3_n, C1 |
| 21 | DQ14 | 165 | VSS | 94 | VSS | 238 | SA2 |
| 22 | VSS | 166 | DQ15 | 95 | DQ36 | 239 | VSS |
| 23 | DQ10 | 167 | VSS | 96 | VSS | 240 | DQ37 |
| 24 | VSS | 168 | DQ11 | 97 | DQ32 | 241 | VSS |
| 25 | DQ20 | 169 | VSS | 98 | VSS | 242 | DQ33 |
| 26 | VSS | 170 | DQ21 | 99 | TDQS13_t, DQS13_t, DM4_n, DBI4_n, NC | 243 | VSS |
| 27 | DQ16 | 171 | VSS | 100 | TDQS13_c, DQS13_c, NC | 244 | DQS4_c |
| 28 | VSS | 172 | DQ17 | 101 | VSS | 245 | DQS4_t |
| 29 | TDQS11_t, DQS11_t, DM2_n, DBI2_n, NC | 173 | VSS | 102 | DQ38 | 246 | VSS |
| 30 | TDQS11_c, DQS11_c, NC | 174 | DQS2_c | 103 | VSS | 247 | DQ39 |
| 31 | VSS | 175 | DQS2_t | 104 | DQ34 | 248 | VSS |
| 32 | DQ22 | 176 | VSS | 105 | VSS | 249 | DQ35 |
| 33 | VSS | 177 | DQ23 | 106 | DQ44 | 250 | VSS |
| 34 | DQ18 | 178 | VSS | 107 | VSS | 251 | DQ45 |
| 35 | VSS | 179 | DQ19 | 108 | DQ40 | 252 | VSS |
| 36 | DQ28 | 180 | VSS | 109 | VSS | 253 | DQ41 |
| 37 | VSS | 181 | DQ29 | 110 | TDQS14_t, DQS14_t, DM5_n, DBI5_n, NC | 254 | VSS |
| 38 | DQ24 | 182 | VSS | 111 | TDQS14_c, DQS14_c, NC | 255 | DQS5_c |
| 39 | VSS | 183 | DQ25 | 112 | VSS | 256 | DQS5_t |

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|---------------------------------------|---------|----------|---------|--------------------------------------|---------|----------|
| 40 | TDQS12_t, DQS12_t, DM3_n, DBI3_n4, NC | 184 | VSS | 113 | DQ46 | 257 | VSS |
| 41 | TDQS12_c, DQS12_c, NC | 185 | DQS3_c | 114 | VSS | 258 | DQ47 |
| 42 | VSS | 186 | DQS3_t | 115 | DQ42 | 259 | VSS |
| 43 | DQ30 | 187 | VSS | 116 | VSS | 260 | DQ43 |
| 44 | VSS | 188 | DQ31 | 117 | DQ52 | 261 | VSS |
| 45 | DQ26 | 189 | VSS | 118 | VSS | 262 | DQ53 |
| 46 | VSS | 190 | DQ27 | 119 | DQ48 | 263 | VSS |
| 47 | CB4, NC | 191 | VSS | 120 | VSS | 264 | DQ49 |
| 48 | VSS | 192 | CB5, NC | 121 | TDQS15_t, DQS15_t, DM6_n, DBI6_n, NC | 265 | VSS |
| 49 | CB0, NC | 193 | VSS | 122 | TDQS15_c, DQS15_c, NC | 266 | DQS6_c |
| 50 | VSS | 194 | CB1, NC | 123 | VSS | 267 | DQS6_t |
| 51 | TDQS17_t, DQS17_t, DM8_n, DBI8_n, NC | 195 | VSS | 124 | DQ54 | 268 | VSS |
| 52 | TDQS17_c, DQS17_c, NC | 196 | DQS8_c | 125 | VSS | 269 | DQ55 |
| 53 | VSS | 197 | DQS8_t | 126 | DQ50 | 270 | VSS |
| 54 | CB6, NC | 198 | VSS | 127 | VSS | 271 | DQ51 |
| 55 | VSS | 199 | CB7, NC | 128 | DQ60 | 272 | VSS |
| 56 | CB2, NC | 200 | VSS | 129 | VSS | 273 | DQ61 |
| 57 | VSS | 201 | CB3, NC | 130 | DQ56 | 274 | VSS |
| 58 | RESET_n | 202 | VSS | 131 | VSS | 275 | DQ57 |
| 59 | VDD | 203 | CKE1, NC | 132 | TDQS16_t, DQS16_t, DM7_n, DBI7_n, NC | 276 | VSS |
| 60 | CKE0 | 204 | VDD | 133 | TDQS16_c, DQS16_c, NC | 277 | DQS7_c |
| 61 | VDD | 205 | RFU | 134 | VSS | 278 | DQS7_t |
| 62 | ACT_n | 206 | VDD | 135 | DQ62 | 279 | VSS |
| 63 | BG0 | 207 | BG1 | 136 | VSS | 280 | DQ63 |
| 64 | VDD | 208 | ALERT_n | 137 | DQ58 | 281 | VSS |
| 65 | A12/BC_n | 209 | VDD | 138 | VSS | 282 | DQ59 |
| 66 | A9 | 210 | A11 | 139 | SA0 | 283 | VSS |
| 67 | VDD | 211 | A7 | 140 | SA1 | 284 | VDDSPD |
| 68 | A8 | 212 | VDD | 141 | SCL | 285 | SDA |
| 69 | A6 | 213 | A5 | 142 | VPP | 286 | VPP |
| 70 | VDD | 214 | A4 | 143 | VPP | 287 | VPP |
| 71 | A3 | 215 | VDD | 144 | RFU | 288 | VPP |
| 72 | A1 | 216 | A2 | | | | |
| 73 | VDD | 217 | VDD | | | | |

1. Light colored text indicates functions that are not applicable for RDIMM wiring. An example is the NC for pin 56 because RDIMMs defined by this specification will always have DIMM wiring for this pin.

*IC Component Composition :

| | | | |
|---------|---------|---------|--------|
| 256Mx8 | A0~A13 | 512Mx4 | A0~A14 |
| 512Mx8 | A0~A14, | 1024Mx4 | A0~A15 |
| 1024Mx8 | A0~A15, | 2048Mx4 | A0~A16 |
| 2048Mx8 | A0~A16, | | |

Pin Descriptions

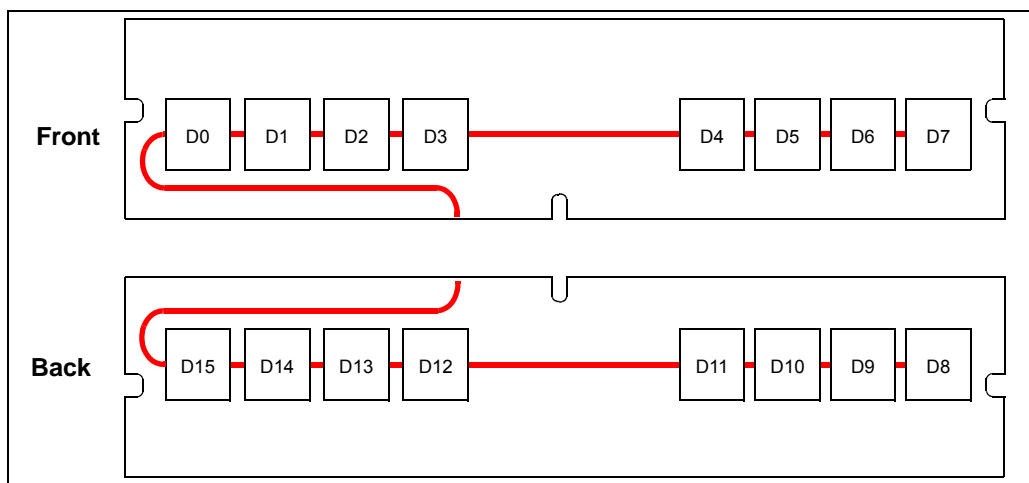
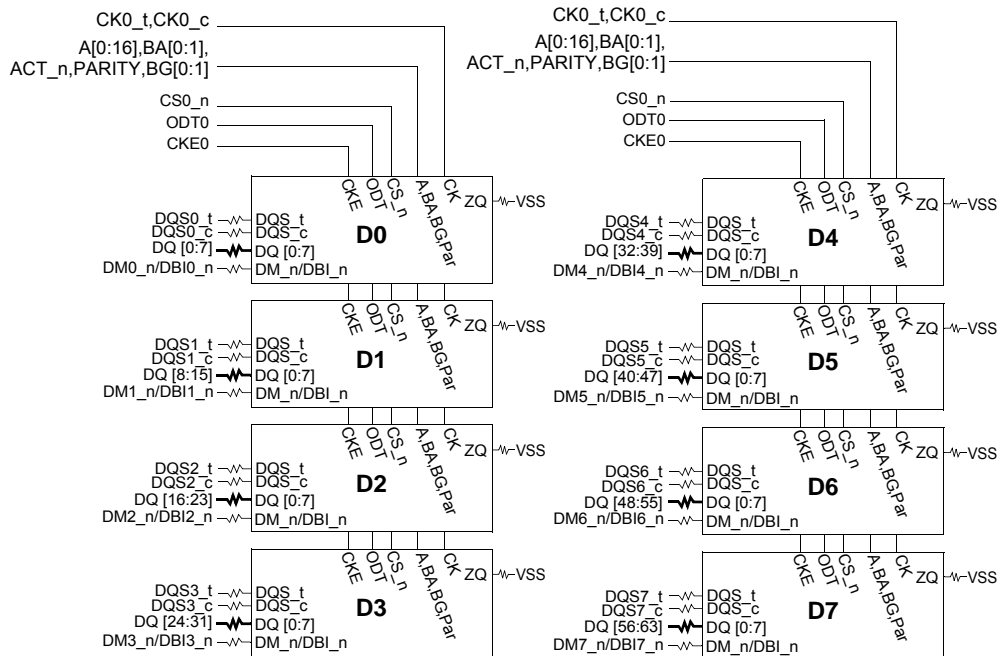
| Pin Name | Description |
|---------------------|---|
| Ax ^{1*} | SDRAM address bus |
| BAx | SDRAM bank select |
| BGx | SDRAM bank group select |
| RAS_n ^{2*} | SDRAM row address strobe |
| CAS_n ^{3*} | SDRAM column address strobe |
| WE_n ^{4*} | SDRAM write enable |
| CSx_n | DIMM Rank Select Lines |
| CKEx | SDRAM clock enable lines |
| ODTx | SDRAM on-die termination control lines |
| ACT_n | SDRAM input for activate input |
| DQx | DIMM memory data bus |
| CBx | DIMM ECC check bits |
| TDQSx_t ; TDQSx_c | Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs |
| DQSx_t | Data Buffer data strobes (positive line of differential pair) |
| DQSx_c | Data Buffer data strobes (negative line of differential pair) |
| DMx_n, DBlx_n | SDRAM data masks/data bus inversion(x8-based x72 DIMMs) |
| CKx_t | SDRAM clock input (positive line of differential pair) |
| CKx_c | SDRAM clocks input (negative line of differential pair) |
| SCL | I ² C serial bus clock for SPD-TSE and register |
| SDA | I ² C serial bus data line for SPD-TSE and register |
| SAX | I ² C slave address select for SPD-TSE and register |
| PARITY | SDRAM parity input |
| VDD | SDRAM core power supply |
| 12 V | Optional Power Supply on socket but not used on DIMM |
| VREFCA | SDRAM command/address reference supply |
| VSS | Power supply return (ground) |
| VDDSPD | Serial SPD-TSE positive power supply |
| ALERT_n | SDRAM ALERT_n output |
| VPP | SDRAM Supply |
| RESET_n | Set Register and SDRAMs to a Known State |
| EVENT_n | SPD signals a thermal event has occurred |
| VTT | SDRAM I/O termination supply |
| RFU | Reserved for future use |

*Notes:

1. Address A17 is only valid for 16 Gb x4 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Functional Block Diagram

Part 1 of 2

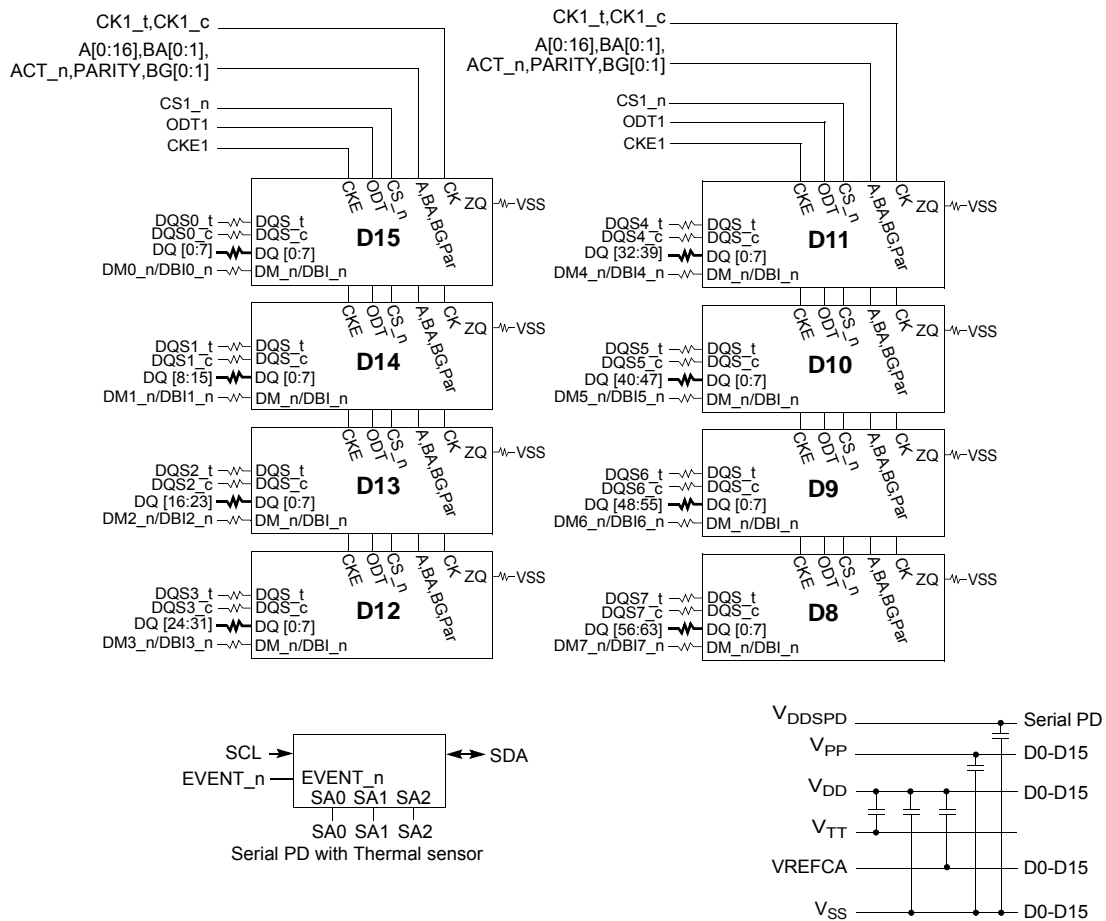


— Address, Command and Control lines

Note 1: Unless otherwise noted, resistor values are $15\Omega \pm 5\%$.

Note 2: ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Part 2 of 2



Note 1: Unless otherwise noted, resistor values are $15\Omega \pm 5\%$.

Note 2: ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 3: For part 2 of 2 the DQ resistors are shown for simplicity but are the same physical components as shown on part 1 of 2.

Note 4: EVENT_n is wired on this design. A standalone SPD may be used as well. No wiring changes are required.

Absolute Maximum Ratings

| Parameter | Symbol | Description | Units | Notes |
|-------------------------------------|-------------------|-----------------|-------|-------|
| Voltage on VDD pin relative to Vss | V_{DD} | - 0.3 V ~ 1.5 V | V | 1,3 |
| Voltage on VDDQ pin relative to Vss | V_{DDQ} | - 0.3 V ~ 1.5 V | V | 1,3 |
| Voltage on VPP pin relative to Vss | V_{PP} | - 0.3 V ~ 3.0 V | V | 4 |
| Voltage on any pin relative to Vss | V_{IN}, V_{OUT} | - 0.3 V ~ 3.0 V | V | 1 |
| Storage Temperature | T_{STG} | -55 to +100 | °C | 1,2 |

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times

DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Units | Notes |
|--------|------------------------------------|----------|-------|-------|
| TOPER | Normal Operating Temperature Range | 0 to 85 | °C | 1,2 |
| | Extended Temperature Range | 85 to 95 | °C | 1,3 |

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
 - b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

Operating Conditions

Recommended DC Operating Conditions – DDR4 (1.2V) operation

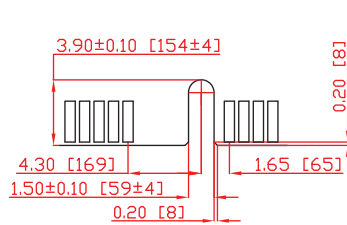
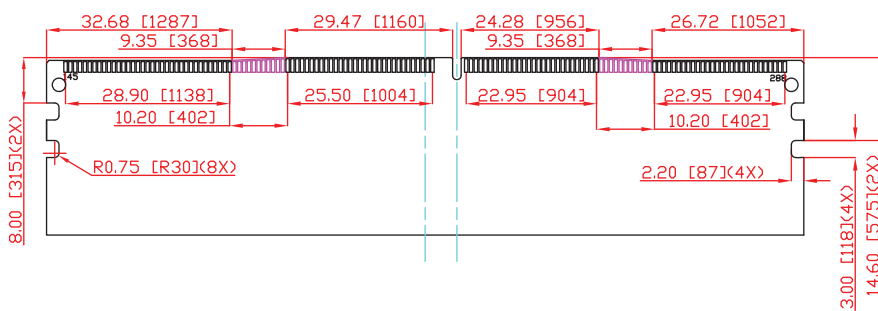
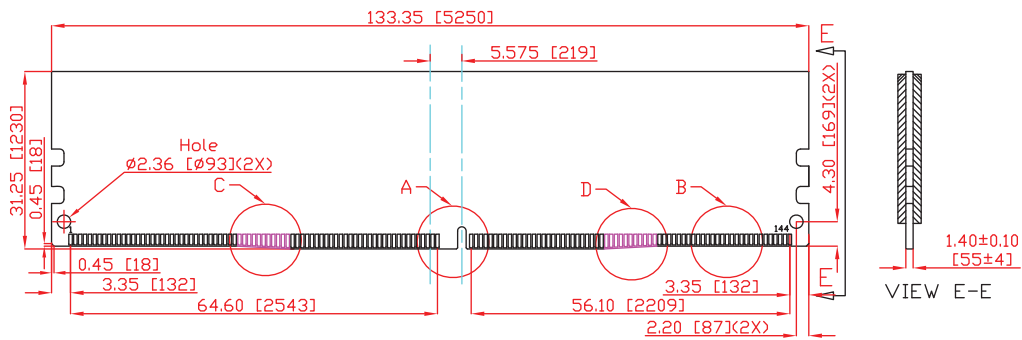
| Symbol | Parameter | Rating | | | Units | Notes |
|--------|---------------------------|--------|------|------|-------|-------|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VDDQ | Supply Voltage for Output | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VPP | | 2.375 | 2.5 | 2.75 | V | 3 |

Notes:

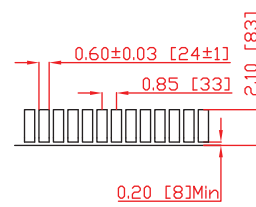
1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

Mechanical Drawing

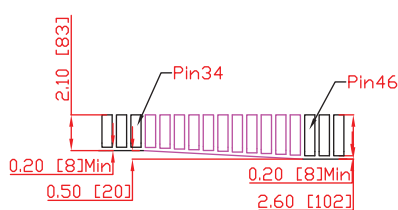
Unit: mm



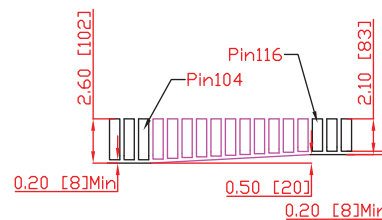
Detail A



Detail B



Detail C



Detail D

(All dimensions are in millimeters with ± 0.15 mm tolerance unless specified otherwise.)

Revision History

| Revision | Date | Description | Remark |
|-----------------|-------------|--------------------|---------------|
| 0.1 | 5/5/2014 | Initial release | |
| 0.2 | 11/2/2015 | Updated VDDSPD | |

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist.,

New Taipei City 236, Taiwan R.O.C.

Tel: +886-2-2267-8000

Fax: +886-2-2267-2261

amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.

46732 Lakeview Blvd., Fremont, CA 94538

Tel: 1-408-518-8699

Fax: 1-510-249-9568

sa@apacerus.com

Japan

Apacer Technology Corp.

5F, Matsura Bldg., Shiba, Minato-Ku

Tokyo, 105-0014, Japan

Tel: 81-3-5419-2668

Fax: 81-3-5419-0018

jpservices@apacer.com

Europe

Apacer Technology B.V.

Science Park Eindhoven 5051 5692 EB Son,

The Netherlands

Tel: 31-40-267-0000

Fax: 31-40-290-0686

sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd.

Room D, 22/FL, No.2, Lane 600, Jieyun Plaza,

Tianshan RD, Shanghai, 200051, China

Tel: 86-21-6228-9939

Fax: 86-21-6228-9936

sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd.

Unit No.201, "Brigade Corner", 7th Block Jayanagar,

Yediyur Circle, Bangalore – 560082, India

Tel: 91-80-4152-9061

Fax: 91-80-4170-0215

sales_india@apacer.com