RoHS Compliant

2GB ECC Registered DDR2 SO-DIMM

Product Specifications

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Version 1.1

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General Description

Apacer **78.A2G80.4000C** is 256M x 72 bit DDR2 SDRAM (Synchronous DRAM) Small-Outline Registered Dual In-line Memory Module (SORDIMM).

It consists of 18 pieces 128M x 8 bit with 8banks Double Data Rate SDRAMs in 60Ball FBGA packages mounted on a 200pin glass-epoxy substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
78.A2G80.4000C	5.3 GB/sec	667 Mbps	333 MHz	CL5

Density	Organization	Component	Rank
2GB	256M x 72	128M x8*18	2

Key Parameters

MT/s	DDR2-667	DDR2-800	DDR2-800	Unit
Grade	-CL5	-CL5	-CL6	
tCK (min)	3	2.5	2.5	ns
CAS latency	5	5	6	tCK
tRCD (min)	15	12.5	15	ns
tRP (min)	15	12.5	15	ns
tRAS (min)	45	45	45	ns
tRC (min)	60	57.5	60	ns
CL-tRCD-tRP	5-5-5	5-5-5	6-6-6	tCK

Specifications:

- Support ECC error detection and correction
- JEDEC standard 1.8V ± 0.1V
- Power Supply VDDQ = 1.8V± 0.1V
- Interface: SSTL_18
- Posted CAS
- Programmable CAS Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3, 4
- Write Latency (WL) = Read Latency (RL) -1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Refresh and Self Refresh

  Average Refresh Period 7.8us
- Serial presence detect with EEPROM
- Compliance with RoHS
- Compliance with CE
- Supports auto-refresh/self-refresh
- Operating Temperature Range:

  Commercial 0°C≦TC≦85°C
- Average refresh period

  7.8us at 0°C ≦ TC ≦ 85°C

  3.9us at 85°C ≦ TC ≦ 95°C

Pin Assignments

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	2	Vss	51	DQ18	52	Vss
3	DQ0	4	DQ4	53	DQ19	54	DQ28
5	Vss	6	DQ5	55	Vss	56	DQ29
7	DQ1	8	Vss	57	DQ24	58	VSS
9	$\overline{\text{DQS0}}$	10	DM0	59	DQ25	60	DM3
11	DQS0	12	Vss	61	Vss	62	Vss
13	Vss	14	DQ6	63	$\overline{\text{DQS3}}$	64	DQ30
15	DQ2	16	DQ7	65	DQS3	66	DQ31
17	DQ3	18	Vss	67	Vss	68	Vss
19	Vss	20	DQ12	69	DQ26	70	CB4
21	DQ8	22	DQ13	71	DQ27	72	CB5
23	DQ9	24	Vss	73	Vss	74	Vss
25	Vss	26	DM1	75	CB0	76	DM8
27	$\overline{\text{DQS1}}$	28	Vss	77	CB1	78	Vss
29	DQS1	30	DQ14	79	Vss	80	CB6
31	Vss	32	DQ15	81	$\overline{\text{DQS8}}$	82	CB7
33	DQ10	34	Vss	83	DQS8	84	Vss
35	DQ11	36	DQ20	85	Vss	86	CB2
37	Vss	38	DQ21	87	CKE0	88	CB3
39	DQ16	40	Vss	89	NC/ CKE1	90	Vss
41	DQ17	42	$\overline{\text{RESET}}$	91	NC/ $\overline{\text{S2}}$	92	NC/ BA2
43	Vss	44	DM2	93	VDD	94	NC/ A14
45	$\overline{\text{DQS2}}$	46	Vss	95	A12	96	A11
47	DQS2	48	DQ22	97	A9	98	VDD
49	Vss	50	DQ23	99	A7	100	A8

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
101	VDD	102	A6	151	VSS	152	VSS
103	A5	104	A4	153	$\overline{\text{DQS5}}$	154	DM5
105	A3	106	VDD	155	DQS5	156	VSS
107	A2	108	A1	157	VSS	158	DQ46
109	VDD	110	A0	159	DQ42	160	DQ47
111	A10 / AP	112	BA1	161	DQ43	162	VSS
113	BA0	114	VDD	163	VSS	164	DQ52
115	$\overline{\text{RAS}}$	116	$\overline{\text{WE}}$	165	DQ48	166	DQ53
117	VDD	118	$\overline{\text{S0}}$	167	DQ49	168	VSS
119	$\overline{\text{CAS}}$	120	ODT0	169	VSS	170	DM6
121	NC/ $\overline{\text{S1}}$	122	NC/ A13	171	$\overline{\text{DQS6}}$	172	VSS
123	VDD	124	VDD	173	DQS6	174	DQ54
125	NC/ ODT1	126	CK0	175	VSS	176	DQ55
127	NC/ $\overline{\text{S3}}$	128	$\overline{\text{CK0}}$	177	DQ50	178	VSS
129	DQ32	130	VSS	179	DQ51	180	DQ60
131	VSS	132	DQ36	181	VSS	182	DQ61
133	DQ33	134	DQ37	183	DQ56	184	VSS
135	$\overline{\text{DQS4}}$	136	VSS	185	DQ57	186	DM7
137	DQS4	138	DM4	187	VSS	188	DQ62
139	VSS	140	VSS	189	$\overline{\text{DQS7}}$	190	VSS
141	DQ34	142	DQ38	191	DQS7	192	DQ63
143	DQ35	144	DQ39	193	DQ58	194	SDA
145	VSS	146	VSS	195	VSS	196	SCL
147	DQ40	148	DQ44	197	DQ59	198	SA1
149	DQ41	150	DQ45	199	VDDSPD	200	SA0

Notes:

1. NC/ $\overline{\text{S2}}$, NC/ $\overline{\text{S3}}$ (Pin 91, 127) are used for 4 rank DIMMs..
2. $\overline{\text{RESET}}$ (Pin 42) $\overline{\text{RESET}}$ is connected to OE of the PLL.

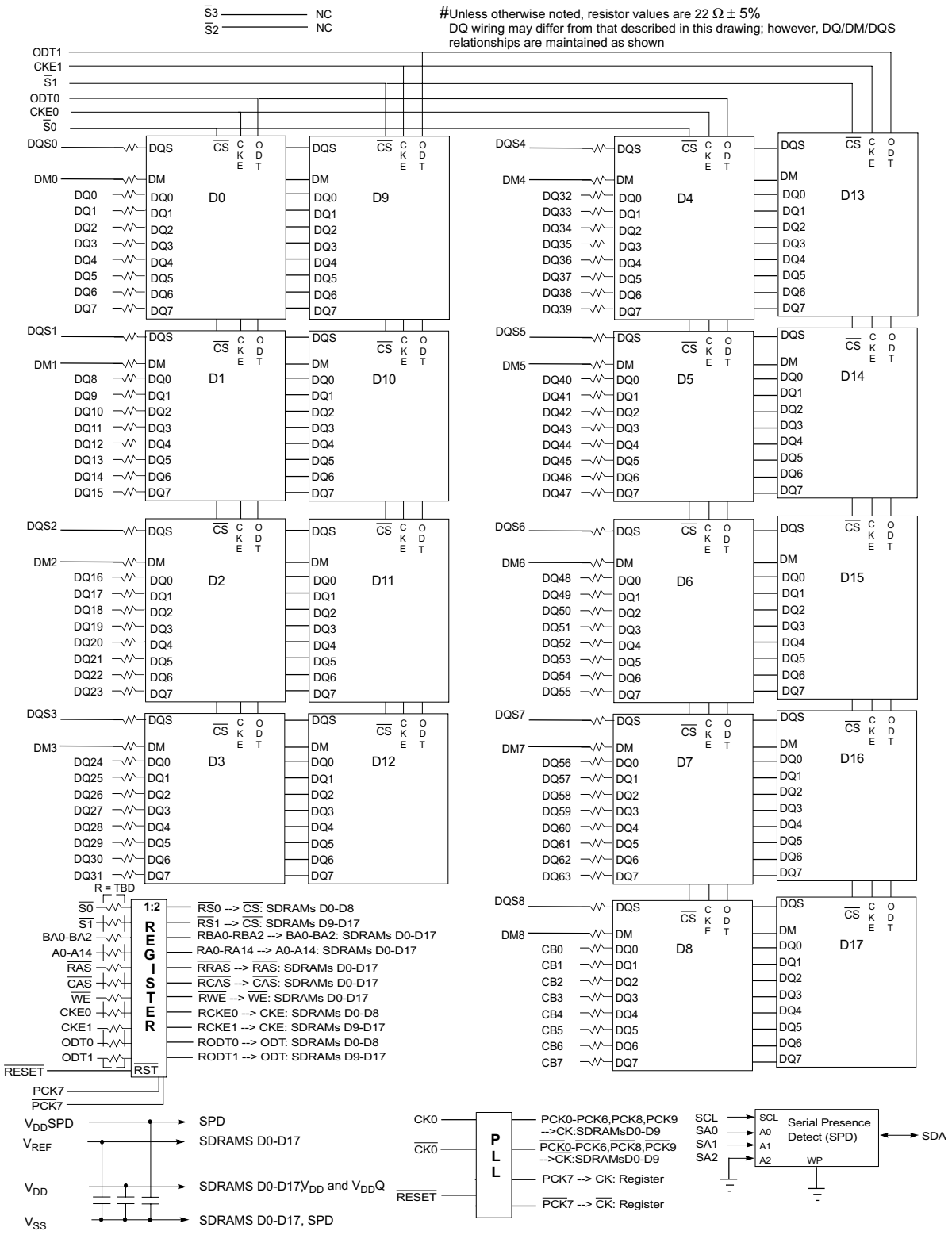
Pin Descriptions

Pin Name	Description
Ax	SDRAM address bus
BAx	SDRAM bank select
$\overline{RAS}$	SDRAM row address strobe
$\overline{CAS}$	SDRAM column address strobe
$\overline{WE}$	SDRAM write enable
$\overline{Sx}$	DIMM Rank Select Lines
CKEx	SDRAM clock enable lines
ODTx	On-die termination control lines
DQx	DIMM memory data bus
CBx	DIMM ECC check bits
DQSx	SDRAM data strobes(positive line of differential pair)
$\overline{DQSx}$	SDRAM data strobes(negative line of differential pair)
DMx	SDRAM data masks high data strobes(x8-based X72 DIMMs)
CKx	SDRAM clocks(positive line of differential pair)
$\overline{CKx}$	SDRAM clocks(negative line of differential pair)
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data line for EEPROM
SAx	I2C slave address select for EEPROM
V_{DD}	SDRAM core power supply
V_{REF}	SDRAM I/O reference supply
V_{SS}	Power supply return(ground)
V_{DD}SPD	Serial EEPROM positive power supply
NC	Spare pins(no connect)
RESET	Set DRAMs to Known State

Notes:

1. A13 is used for x4/x8 base Un-buffered DIMM..

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Description	Units
Voltage on VDD pin relative to Vss	V_{DD}	- 1.0 V ~ 2.3 V	V
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.5 V ~ 2.3 V	V
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.5 V ~ 2.3 V	V
Storage Temperature	TSTG	-55 to +100	℃

Notes:

2. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability..
3. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard
4. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ. When VDD and VDDQ and VDDL are less than 500mV, VREF may be equal to or less than 300mV.4. Voltage on any input or I/O may not exceed voltage on VDDQ..

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DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Operating Temperature Range	0 to 85	℃	1,2
	Extended Temperature Range	85 to 95	℃	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For Measurement conditions please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported During operation, the DRAM case temperature must be maintained between 0 - 85℃ under all operating Conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85℃ and 95℃ case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
    a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability.
    b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 =1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b.

Operating Conditions

Recommended DC Operating Conditions – DDR2 (1.8V) operation

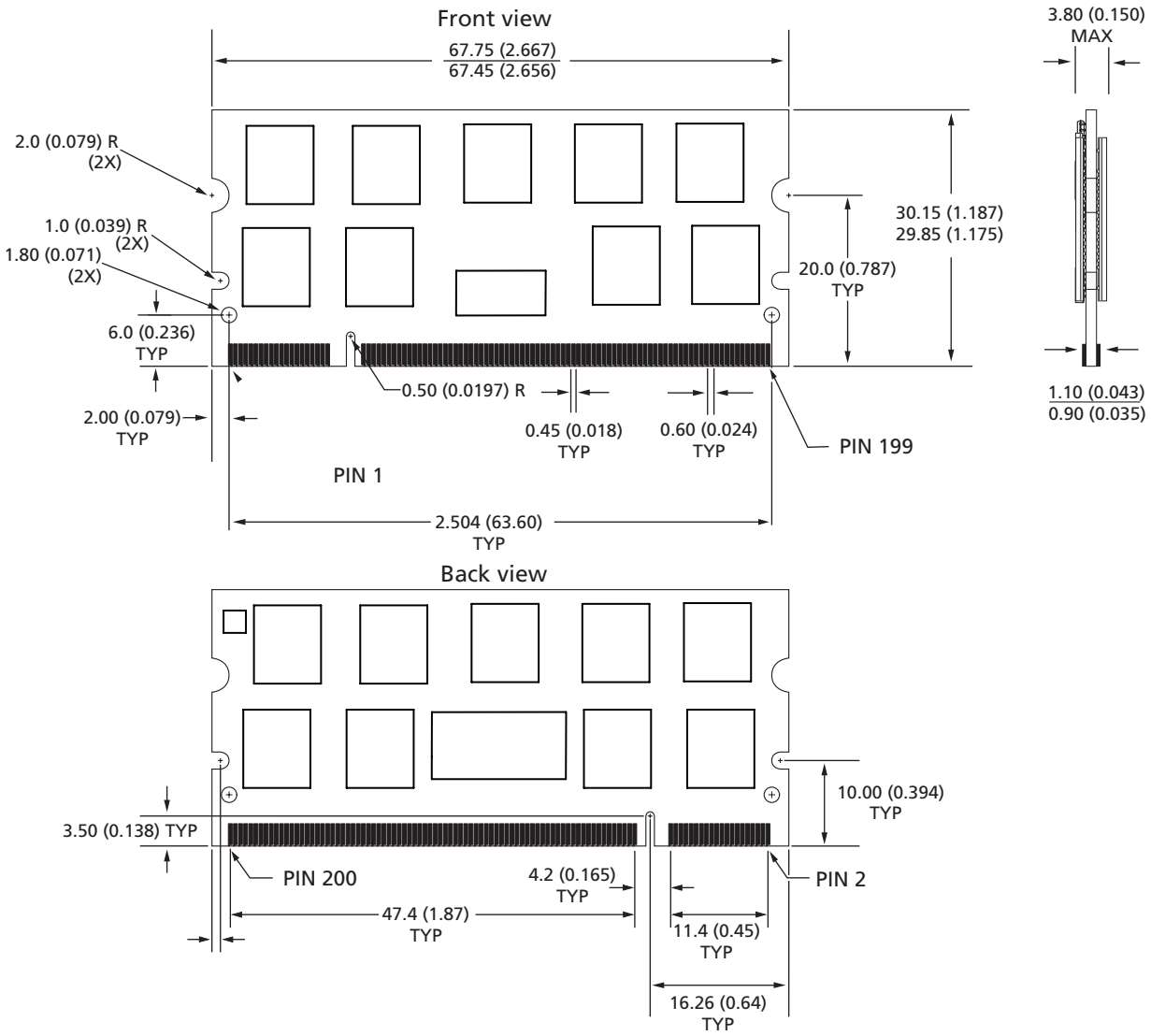
Symbol	Parameter	Rating			Units
		Min.	Typ.	Max.	
VDD	Supply Voltage	1.7	1.8	1.9	V
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V

Notes:

1. There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD..
2. AC parameters are measured with VDD, VDDQ and VDDL tied together..

Mechanical Drawing

Unit: mm



Tolerances:+-0.15mm unless otherwise specified

Revision History

Revision	Date	Description	Remark
0.9	08/28/2012	Official release	
1.0	08/29/2012	release	
1.1	07/23/2013	1. Changed headquarters address 2. Added 30µ gold finger	

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